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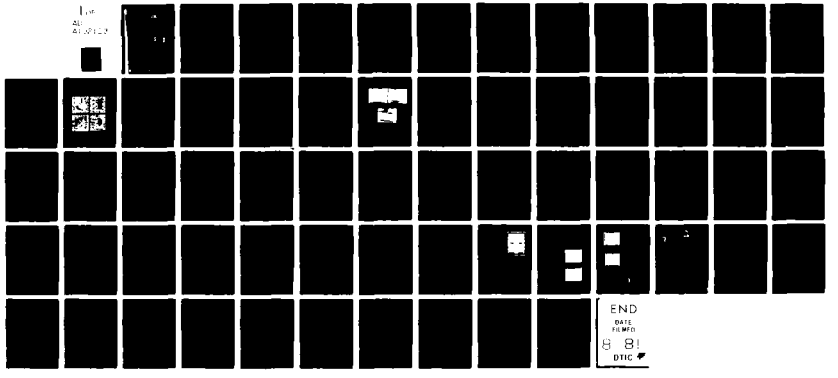

LEVEL II

(1)

RADIATION-HARDENED N^+ GATE CMOS/SOS

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Process development work for a hardened N^+ polysilicon-gate CMOS/SOS process has demonstrated that it is possible to make functional 4K CMOS/SOS static RAMs that are hard to 5×10^5 rads without the implementation of special hardened circuit design techniques.

Present circuit probe yields are low, limited by the lack of a hardened low-temperature contoured field oxide. Independent research

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has shown that a hardened reflow process is possible for such field oxides. Development of this reflow process is nearly complete and should result in significant improvement in yields when fully integrated into the rad-hard N^+ process.

PREFACE

This report, prepared by RCA Laboratories, Princeton, New Jersey, under Contract N00014-78-C-0891, describes work preformed principally in the Integrated Circuit Technology Research Laboratory, D. E. O'Connor, Director.

The project scientist is G. W. Hughes. G. J. Brucker and R. K. Smeltzer helped design processing experiments and test the resulting circuits. S. T. Hsu contributed to the ion-implantation experimental design. Device processing was performed by the SOS pilot-line staff at RCA Solid State Technology Center, Somerville, New Jersey. The assistance of S. G. Policastro is especially appreciated.

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SECTION I

INTRODUCTION

This is the final report for Phases I and II of Naval Research Laboratories (DNA sponsored) contract N00014-78-C-0891, entitled "Radiation-Hard n^+ Gate CMOS/SOS." The objective of this program is to develop n^+ silicon-gate complementary metal-oxide-semiconductor/silicon-on-sapphire (CMOS/SOS) processing techniques for the high-yield fabrication of large-scale integrated (LSI/VLSI) circuits with a broad range of functional capabilities, including random logic and memory. The program consisted of three phases. The objectives of Phase I, a 5-month effort, were to define and develop a radiation-hardened n^+ silicon-gate CMOS/SOS process for a small-scale integration (SSI) array. In Phase II, a 4-month effort, RCA evaluated the process developed in Phase I, using LSI test vehicles (including LSI design rule vehicles), and a 4K random-access memory (RAM). This evaluation included electrical and radiation testing.

During Phase III RCA will continue development of the n^+ gate rad-hard process, but will concentrate on efforts in two areas: (1) thin-oxide, short-channel devices and (2) edge and back-channel leakage problems.

Silicon-gate CMOS/SOS is a technology that offers significant advantages for certain military semiconductor applications because of its low power consumption; high speed; high packing density; and inherent radiation hardness in terms of latch-up, transient upset, and single events. Like many other commercial processes the commercial Si-gate process is very sensitive to total-dose radiation. To achieve any degree of total-dose radiation hardness a processing technology must use low-temperature oxides without ever exceeding the oxidation temperature in subsequent processing steps. Typical processing steps in which post-oxidation high temperatures are ordinarily used are the implant-activation step and the contoured field-oxide operation. Replacement of these processes with lower-temperature steps invariably has, in most cases, an adverse impact on both circuit performance (speed) and yield.

Circuit speed of CMOS is affected by the current-gain of the transistors, as well as threshold voltages and interconnect resistivity. Implementation of a rad-hard Si-gate process has the greatest effect on threshold voltage and interconnect resistivity. N-channel threshold voltages (V_{TN}) are increased so that the devices do not become depletion-mode devices as radiation shifts the

threshold in a negative direction. This larger V_{TN} compromises speed. The polysilicon interconnect resistivity for the reduced-temperature process is large because the post-oxidation processing-step temperatures are too low to fully activate the dopant. This also compromises speed.

The differences in circuit yield between a commercial and a rad-hard process are due primarily to metal step-coverage problems. The high temperatures needed to establish a good contoured field-oxide are detrimental to radiation hardness. Consequently no contoured oxide is used and yields are correspondingly reduced.

The goal of radiation-hardened process development then is to establish a degree of harmony between radiation hardness on the one hand and speed and yield on the other. Much of the early work in this area concentrated on a p^+ gate technology. However, p^+ polysilicon has too high a sheet resistivity for many high-speed applications. Also, it has been susceptible to room-temperature instability problems in the past. The present work is an attempt to develop an n^+ Si-gate technology that will eliminate both of these problems.

SECTION II

SCOPE AND OBJECTIVES

A. PROCESS DEVELOPMENT FOR THE n^+ GATE

Originally, RCA established a hardened process technology using boron-doped p^+ polysilicon gates for CMOS/SOS circuits [1]. This p^+ gate radiation-hardened process has been employed for the fabrication of LSI arrays such as a 292-gate universal array (TCS052), an LSI test cell (TCS059), an 8-bit adder (TCS069), a p-code generator (TCS102), and the Fault Tolerant Computer Test Chip (TCS125). Arrays have operated and satisfied leakage and speed specifications after irradiation to 10^6 rad (Si).

Until now, results comparable to the above achievements in radiation hardening have not been obtained when the hardened process has been modified to fabricate n^+ silicon-gate circuits, which offer the advantage of greater circuit speed. It is not well established why the previous n^+ silicon-gate circuits have not been hard, but, in principle, there is no reason why an n^+ gate process should not produce circuits as radiation-tolerant as p^+ gate circuits. The n^+ gate radiation-hardened process, described below, differs in a number of ways from a conventional CMOS/SOS process, and the particular processing steps that are critical to radiation hardening have been identified.

In the n^+ silicon-gate radiation-hardened CMOS/SOS process, enhancement-mode transistors are fabricated in the manner illustrated in Fig. 1. The key features which lead to radiation tolerance are the low temperatures, the use of all ion-implantation doping, and the radiation-hardened channel oxide.

The CMOS/SOS fabrication process begins with the deposition of a 0.5-μm-thick layer of silicon onto the polished $(1\bar{1}01)$ surface of an annealed sapphire substrate. The silicon is deposited by the pyrolysis of silane (SiH_4). The as-deposited impurity content is almost adequate for the islands of the P-channel devices, so that only a light doping step for the n-islands is used. The silicon islands are formed by a wet anisotropic silicon etch through windows in a grown oxide. The p-islands for the n-channel transistors are then ion-implanted with boron; a photoresist mask is used to shield the n-islands. An anneal is needed after the boron implant.

The gate (channel) oxide is pyrogenically grown, and then annealed in situ.

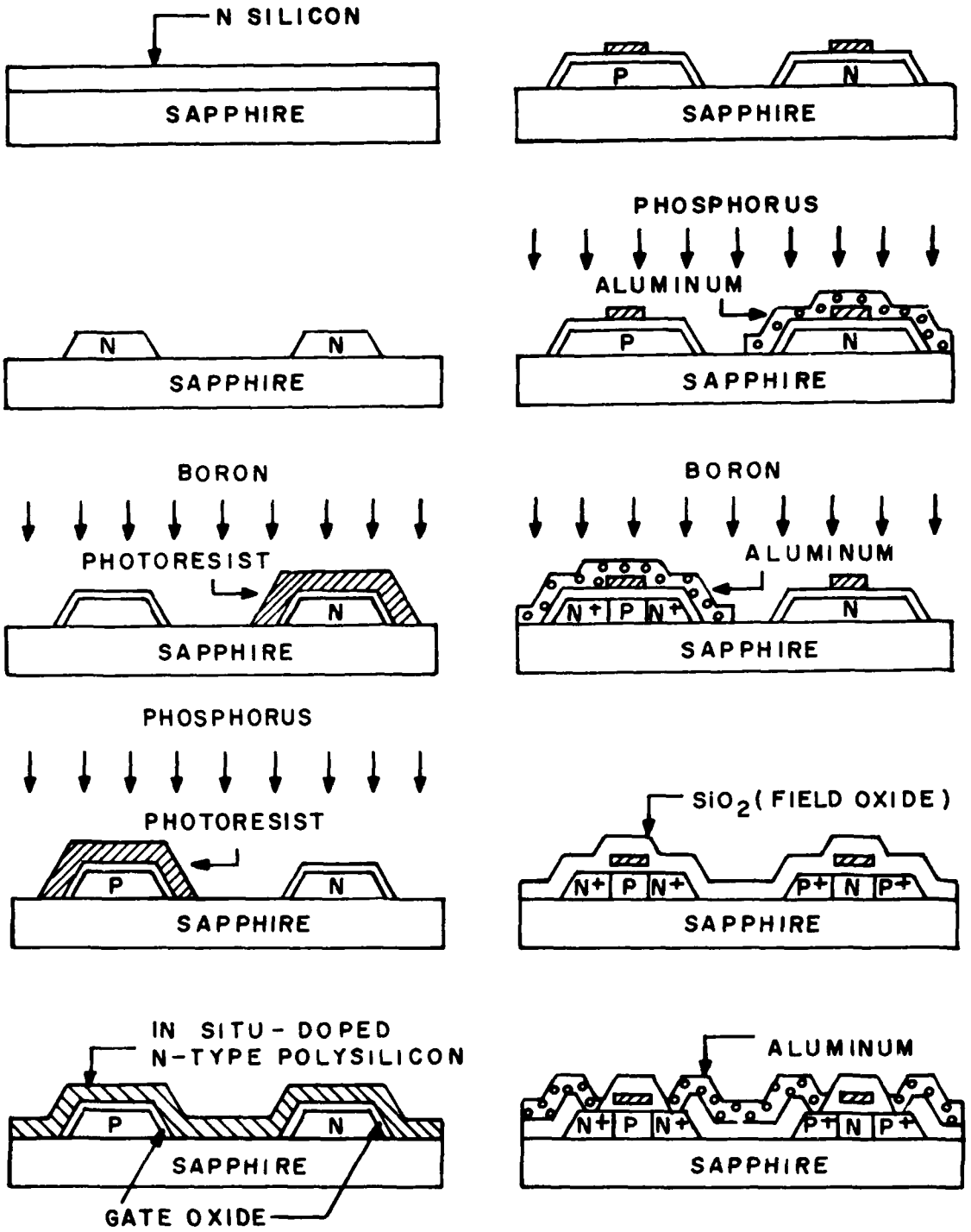


Figure 1. Radiation-hardened n^+ silicon-gate process.

The silicon gate in the n^+ gate process is phosphorus-doped polysilicon deposited onto the gate oxide. In the radiation-hardened process the phosphorus doping is done during deposition to avoid a high-temperature diffusion step. The polysilicon gates are then defined by dry (plasma) or wet chemical etching.

Source and drain self-aligned electrodes are now made. The n-islands (to be used for the p-channel transistors) are shielded, and a phosphorus implant is used to fabricate the n^+ source and drain for the n-channel transistors. In a similar manner, the islands with the now completed n-channel transistors are shielded, and a heavy concentration of boron is implanted to form the p^+ source and drain.

At this point a thick (6000-Å) silicon dioxide film is deposited (at about 350°C) as the field oxide. The source and drain implants are then activated by a low-temperature (850°C) anneal. The contact holes are opened to provide access to the silicon. Induction- or filament-heated aluminum is evaporated and patterned for interconnects. The protective oxide is deposited, and bonding pads are opened to complete the chip fabrication process.

Except for a few modifications the n^+ gate process is very similar to the p^+ gate process. The major differences between the p^+ and n^+ process are in the doping of the polysilicon and the island doping (to compensate for the different barrier heights of n^+ and p^+ poly).

In the n^+ process the silicon gate is doped with phosphorus. The method of the p^+ silicon-gate process, in situ doping during the deposition, can be used; it is also possible to dope the polysilicon by ion implantation, which can be activated during a later oxidation step. However, in situ doping is preferred, since it is completely compatible with a radiation-hardened process and minimizes the number of processing steps. Furthermore, with ion implantation the tail of the ion distribution could be in the gate oxide below the polysilicon. Control wafers are used during the polysilicon deposition, so that the resistivity of the polysilicon can be measured. If the in situ doping does not produce a sufficiently high conductivity, a shallow phosphorus implant into the n-type polysilicon can also be done.

In contrast to the boron-doped silicon-gate process, the phosphorus-doped polysilicon can be patterned by standard wet chemical etchants, as well as by a plasma etching process. This was felt to be another significant positive

feature of the n^+ process, as it was not known if plasma etching affects radiation hardness.

B. TCS099 TEST VEHICLE

The TCS099 A/D converter, shown in Fig. 2, is the process-development vehicle utilized in the Phase I process-development program. This MSI vehicle contains sufficient devices and sufficient accessibility to measure all device characteristics, process parameters, and circuit performance without difficulty. Table 1 is a list of devices included in the TCS099 test vehicle.

C. PHASE I OBJECTIVES

Phase I for this contract consisted of four tasks designed to lead to a radiation-hardened n^+ silicon-gate CMOS/SOS process for an SSI array.

Task 1 is the experimental design. Four lots of 12 wafers each were fabricated with process variations we felt would be most significant in the realization of a radiation-hardened process. Specifically, we evaluated:

1. Ion implantation vs in situ doping of the polysilicon gates.
2. Heated-substrate metal deposition vs cold-metal deposition (to assess yield differences caused by poor metal step-coverage).

In Task 2, suitable numbers of TCS099 arrays from each lot were packaged and radiation-tested (total dose).

Task 3 consisted of the delivery of five packaged parts from each of the four runs to NRL.

Task 4 assessed the process developed in this phase and selected the LSI test vehicles.

D. TCS191 4K RAM

The TCS191 is almost identical to the MWS5114 4K SOS RAM that RCA sells as a commercial part, except that it is approximately 15% larger. (The 5114 is the 191 with a 15% shrink on all dimensions.) A paper describing this circuit is included as an appendix. The chip is organized as 1024 4-bit words and laid out in such a manner that it can be used as a 2K RAM if the full 4K part is not operational.

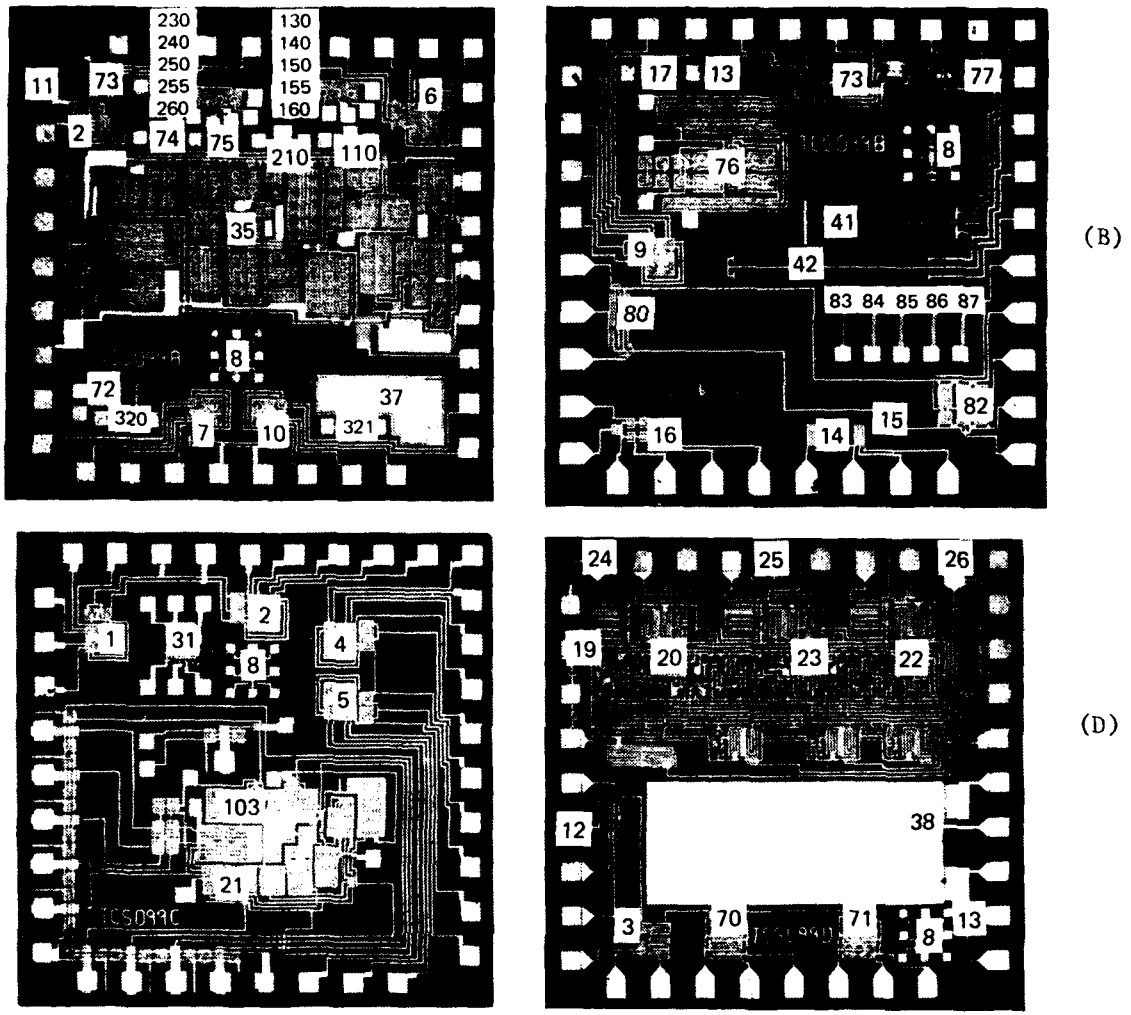


Figure 2. TCS099 A/D converter test chip.

TABLE 1. TCS099 ARRAY CONTENTS (ALL DIMENSIONS IN MIL UNLESS OTHERWISE NOTED)

Chip Location		Function
TCS099A	33	Amplifier
	8	Standard 2-mil test transistors p and n; $L_n = 0.25$, $W_n = 2.0$, $L_p = 2.25$, $W_p = 2.0$
	72	30 minimum area contacts (0.25 mil x 0.25 mil); A = 0.625 mil^2
	320	p epi, L = 6.0, W = 3.2
	321	n epi, L = 6.0, W = 3.2
	37	Poly/metal capacitor, A = 165.60 mil^2
	7	n triplet including a matched pair, L = 0.25, W = 6.0
	10	n triplet including a matched-pair depletion, L = 0.25, W = 6.0
	11	p triplet including a matched-pair depletion, L = 0.25, W = 6.0
	73	p^+ poly resistor, L = 5.8, W = 1.0
	74	Poly step - 20 steps over epi
	75	Metal step - 26 steps over poly
	210	Long-channel n-depletion device, L = 4.0, W = 0.5
	110	Long-channel p-depletion device, L = 3.0, W = 0.5
	6	p triplet including a matched pair, L = 0.3, W = 6.0
	230	Closed n-depletion device, L = 0.3, W = 3.0
	240	Closed n-depletion device, L = 0.4, W = 3.3
	250	Closed n-depletion device, L = 0.5, W = 3.8
	255	Closed n-depletion device, L = 0.55, W = 4.0
	260	Closed n-depletion device, L = 0.6, W = 4.4
	130	Closed p-depletion device, L = 0.3, W = 3.0
	140	Closed p-depletion device, L = 0.4, W = 3.3
	150	Closed p-depletion device, L = 0.5, W = 3.8
	155	Closed p-depletion device, L = 0.55, W = 4.0
	160	Closed p-depletion device, L = 0.6, W = 4.4

TABLE 1. (Cont. -2)

Chip Location		Function
TCS099B	14	Protection zener, W = 4.0
	15	Reference zener, W = 4.0
	82	Closed-geometry oscillator
	80	Standard-geometry oscillator
	9	n triplet with matched pair, clamped, L = 0.25, W = 6.0
	83	p^+ resistor, L = 5.8, W = 0.6
	84	p^+ resistor, L = 5.8, W = 0.3
	85	p^+ resistor, L = 5.8, W = 1.0
	86	n^+ poly, L = 5.8, W = 1.0
	87	p^+ poly, L = 5.8, W = 1.0
	42	2R/2R, L = 32.8, W = 2.0
	41	2R/2R with trim tab, L = 25.2 (11.33 mil^2)
	17	n/n^+ diode, W = 3.2
	18	p/p^+ diode, W. 3.2
	77	T-gate closed geometry, L = 0.3, $W_N = W_P = 3.0$
	78	T-gate standard geometry, L = 0.3, $W_N = W_P = 3.0$
	76	Buffer amplifier
	16	Six-diode switch, W = 3.6
TCS099C	21	Comparator
	103	Isolated input protection
	1	Clamped p triplet with matched pair, L = 0.25, W = 3.4
	31	Cell amplifier
	2	p triplet with matched pair, L = 0.5, W = 7.6
	4	n triplet with matched pair, L = 0.5, W = 7.2
	5	n triplet with matched pair, L = 0.3, W = 6.0
TCS099D	20	SAR input stage
	23	SAR NAND stage
	22	SAR NOR stage
	19	$p\text{-}n^+$ diode pair, W = 36

TABLE 1. (Cont. -3)

Chip Location		Function
TCS099D	24	n epi n^+ diffused resistor, L = 3.6, W = 0.6
	25	n epi n^+ diffused resistor, L = 3.6, W = 0.3
	26	n epi n^+ diffused resistor, L = 3.6, W = 0.9
	12	Inverter standard geometry, $L_p = L_n = 0.25$, $W_p = 9.0$, $W_n = 5.0$
	3	Inverter closed-geometry large device, $L_p = L_n = 0.25$, $W_n = 8.6$, $W_p = 17.2$
	70	Inverter closed-geometry minimum device, $L_p = L_n = 0.25$, $W_n = 9.0$, $W_p = 18.0$
	71	Inverter closed-geometry minimum device, clamped, $L_p = L_n = 0.25$, $W_n = 9.0$, $W_p = 18.0$
	13	Punch-through reference device, L = 0.1
	38	Epi/metal capacitor, A = 523.8 mil^2

NOTES:

Ion-implanted polysilicon resistors (73,86,87) and p^+ epi (83,84,85), n^+ epi (24,25,26), and SiCr resistors (41,42) are to be used to establish resistor value, degree of match, linearity, and power dissipation.

Triplets (6,9,1,2,4,5) are used as matched pairs and in breadboarding tetrodes. These include substrate-clamping test devices.

Zeners have been included (14,15) for protection and reference voltage sources.

E. PHASE II OBJECTIVES

The objectives of Phase II were to assess the n^+ process developed in Phase I to establish a baseline for the radiation tolerance. This process was then to be used to fabricate the TCS191 4K RAM.

SECTION III

RESULTS

A. METAL STEP-COVERAGE YIELD LIMITATIONS

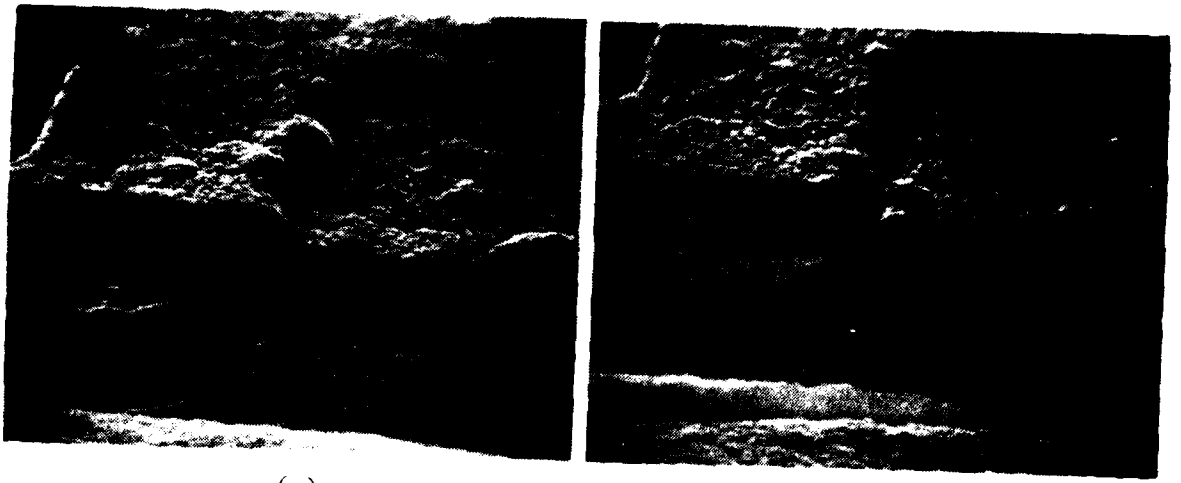
At the present time one of the limiting factors in the yield of radiation-hardened integrated circuits is the yield limitation due to metal step-coverage problems.

In silicon-gate CMOS/SOS circuits metal lines run over polysilicon steps as well as silicon islands. From SEM observations we have concluded that the poly step is usually more severe than the island step and will be the main contributor to a reduction in yield due to step-coverage problems.

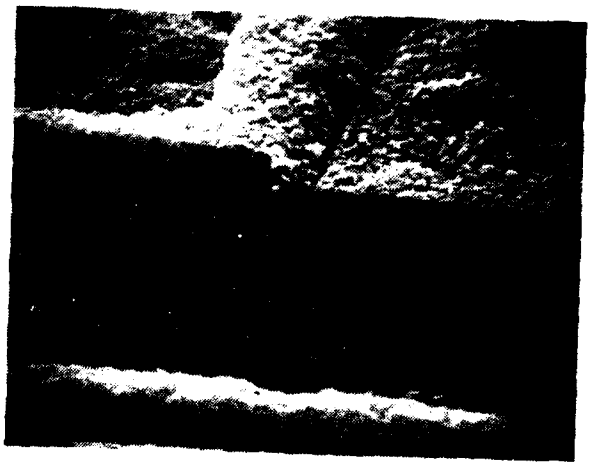
We have investigated metal step-coverage with circuits fabricated with three different metal-deposition conditions. The step coverage shown in the scanning electron photomicrograph of Fig. 3(a) is often observed over steps in the silicon gate after the standard aluminum evaporation onto a room-temperature substrate. What appears is a deep fissure with a constriction in the metal thickness at the step. Figure 3(b) shows the same step from another wafer that had aluminum deposited, but at a wafer temperature of 150°C. Note in particular that the depth of the fissure has been reduced. No significance should be attached to the exact shape in these figures of the step under the metal; the step consists of the polysilicon gate with the field oxide on top, and the field oxide was slightly etched during removal of the SiO_2 overcoat from the chip. Figure 3(c) illustrates the metal step-coverage that was achieved with magnetron-sputtered aluminum from a Varian* S-Gun system. In this case the fissure is very small, and very little constriction of the metal at the step is observed. The results described above suggest two potentially useful techniques, which can be further investigated if we find that improved step coverage is needed.

Although we expect hot metal to have a negligible effect on radiation hardness, it is possible that the sputtered-metal deposition process will degrade the performance of circuits and the radiation tolerance of devices. What we have found is that substrate temperatures near 300°C produce large bias-temperature shifts in capacitors, so that hot metal is not a viable means of providing good metal step coverage.

*Varian Associates, Palo Alto, CA.



(a) (b)



(c)

Figure 3. Scanning electron micrographs of metal steps over polysilicon (10K magnification, 70° angle of incidence). (a) Cold In-source aluminum; (b) hot (150°C) In-source aluminum and; (c) S-Gun aluminum.

However, the use of magnetron-sputtered aluminum yields the best metal step-coverage.

The only drawback to magnetron-sputtered Al is that, under certain conditions, it can produce radiation damage. These conditions occur when the ultraviolet radiation from the sputtering plasma is able to impinge upon the bare SiO_2. More specifically, what is needed to produce radiation damage is that photons of 8-eV or greater energy levels are able to strike the SiO_2 gate insulator. The use of polysilicon gates makes this virtually impossible. Photons with energies of $\geq$8 eV are strongly absorbed by polysilicon, while visible and infrared photons that can penetrate the poly are not energetic enough to create hole-electron pairs in the SiO_2. The postirradiation data from lot 2314 and all other lots we have irradiated bear this out. These lots are just as hard as those metallized with filament or In-source Al.

To quantitatively test the step-coverage problems associated with standard In-source metal, a special test structure, specifically designed to give information about step-coverage yield, was processed. This structure is shown in Fig. 4 and is called the process assessment (PAS) array [2]. Listed in Table 2 are the corresponding dimensions for each mask level. The basic concept inherent in this test structure is that the number of effective defects generated by a particular process step which are detrimental to the definition of a particular physical dimension can be determined by sequentially interrogating the defined pattern. For this reason the array is laid out so that an

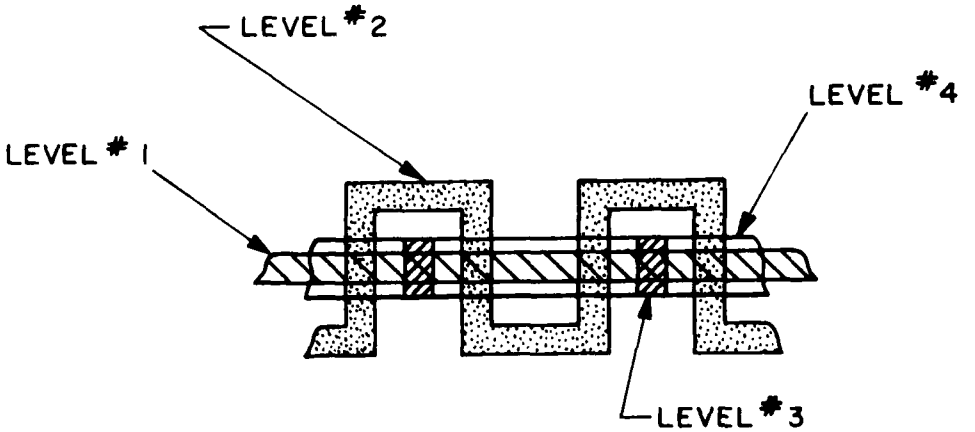


Figure 4. Layout of PAS array test chip.

TABLE 2. PAS TEST-CELL DIMENSIONS

Level No.	Length (mil)	Width (mil)
2	400, 800, 1200, 2400, 4800, 9600, 14400	0.25
4	200, 400, 600, 1300, 2400, 4800, 7200	0.25

increasing number of cells can be analyzed, and a pass or fail condition determined as a function of the number of cells. The number of cells accessible for analysis and brought out to external pads are 200, 400, 600, 1200, 2400, 4800, and 7200. The total array, therefore, contains 14,400 cells. The array dimensions are 170 mil x 200 mil, permitting approximately 100 test chips to be fabricated on a 2-in. (50-mm) wafer. A 3-in. (75-mm) wafer contains about 150 arrays.

The levels listed in Table 2 can be used individually or in various combinations to determine the continuity of different types of conductors or the interaction of one layer with another. Since we were interested only in metal continuity and metal-to-epi as well as metal-to-poly shorts, we used only levels 2 and 4 (0.25-mil metal). The test lot was divided into three experiments. Four wafers were controls - only level 4 (metal) was used. This gives long metal lines on bare sapphire. Four wafers had level 2 (epi) and level 4 (metal). This gives metal over epi that has a gate oxide and field oxide. Four wafers had level 2 (poly) and level 4 (metal). This gives metal over poly with field oxide.

The results of this experiment are shown in Fig. 5. Here we have plotted the yield in percent as a function of the number of crossovers (poly or epi). The individual data points are yield averaged over one wafer. The bands shown represent the yield obtained over the whole lot. Data between 15K crossovers and 40K crossovers are extrapolated.

Since a 4K RAM has approximately 40K crossovers, we can estimate the yield-limiting factor due to no reflow in a 4K RAM from this figure. What the figure shows is that (1) the poly step is the most severe, confirming our earlier observations, and (2) the yield factor due to metal step-coverage problems is only 22-28%. The total yield of the process would be this number multiplied by other yield factors, such as contact continuity yield. Note

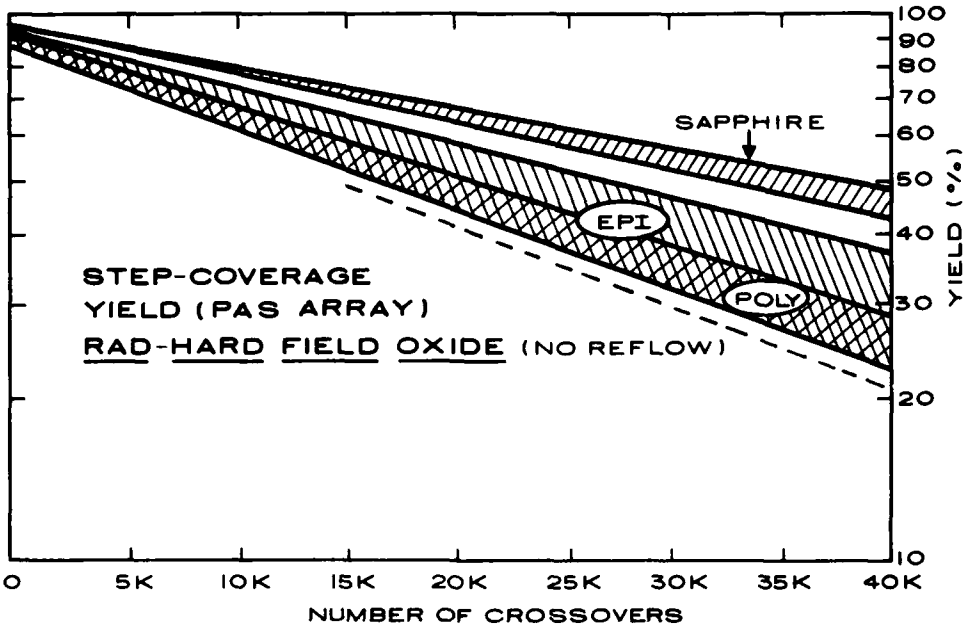


Figure 5. Step-coverage yield as a function of the number of crossovers in the PAS array.

that, without any epi or poly on the wafer, the yield is only 42-50%. Presumably this is caused by such factors as loss by etching or particles on the surface. The use of better metal etching techniques and also a cleaner fabrication facility (soon to be operational) should increase this number. However the "bottom line" in the analysis of this process is that the use of a nonreflowed field oxide is going to limit severely the yield of any rad-hard process. Therefore it is important that future work in this area be directed toward developing a low-temperature contoured field oxide.

B. POLYSILICON DEFINITION

Defining the polysilicon is a critical step in a self-aligned process because the gate is usually of the minimum design-rule width and because that width determines the gain, and thus the circuit speed, of the MOS circuit. N^+ polysilicon is defined by three methods: KOH wet chemical etch, "S-etch",* and plasma etching. For fine geometries plasma etching appears to be the way of

*S-etch is a proprietary RCA wet etchant.

the future, although at the present time not all plasma reactors are equally good for etching. KOH etching is definitely inferior to plasma etching because of undercutting and lifting of the photoresist, but S-etch appears to do a fairly good job in comparison with plasma etching at the present time. For the present work KOH etch and plasma etching were used for the initial runs, but plasma etching, because of its superior etching characteristics, was used for all the later runs that will be reported. Comparative radiation measurements on KOH- and plasma-etched poly devices show no additional degradation in hardness, so we feel that plasma etching is quite compatible with rad-hard processing requirements.

C. POLYSILICON-DOPING TECHNIQUES

Doping of n^+ polysilicon by $POCl_3$ is not permitted in rad-hard processing because of the high temperatures required. The ideal solution would probably be an in situ-doped LPCVD polysilicon process. However, that was not available at the time this work was done. Our best guess as to the most workable solution was to use in situ-doped atmospheric-pressure-CVD polysilicon. Atmospheric CVD does not give totally uniform polysilicon thickness because of the strong dependence of growth rate on temperature and the use of rf-heated susceptors. So, although an atmospheric-pressure-CVD system might give good results with in situ-doped poly, if one were to grow intrinsic poly and then dope it by ion implantation, the nonuniform thickness thus obtained might produce ion penetration into the gate oxide.

Lot #2304 (TCS099) was fabricated to test these different doping schemes. Four wafers received in situ-doped poly (sublot A). Four wafers received intrinsic polysilicon gates, which were then implanted with phosphorus (150 keV, 4.5×10^{15} cm^{-2}) (sublot C). Four received highly in situ-doped poly with the same implant as C (called sublot B). All gates were plasma-etched.

All chips tested were irradiated in the 1-MeV Van de Graaff electron accelerator. In interpreting threshold shifts in the following illustrations, note that these data were obtained from a very high-dose-rate source (10^4 rad/s). Based upon past experience, we expect ^{60}Co threshold shifts to be approximately 60% of the Van de Graaff shifts.

Figure 6 shows preirradiation inverter characteristics for inverter #12 (see Fig. 2) on chips from the three process variations discussed above. All three process variations resulted in less than 1 nA/mil of subthreshold leakage

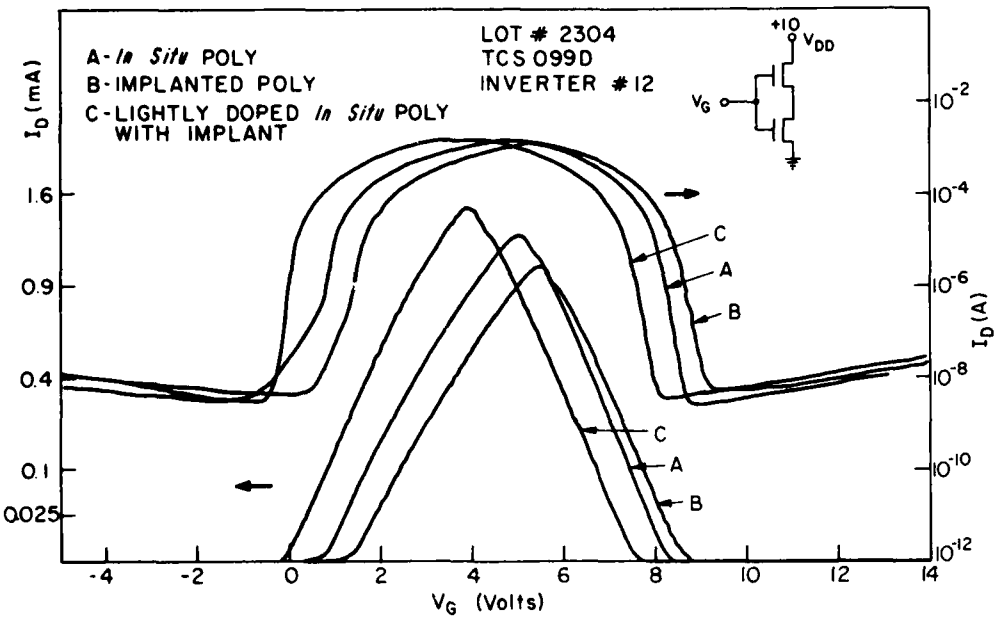


Figure 6. Preirradiation inverter characteristics, I_D vs V_G (I_D plotted on square-root and log scales.)

current. The threshold voltages were designed to be V_{TN} = 2.0 V and V_{TP} = 1.0 V, but as the figure shows, these were not achieved for any of the process variations.

The data from Van de Graaff radiation tests are shown in Figs. 7-9. As these figures show, the poly doped totally in situ and the implanted poly are quite hard and very much harder than the poly that was lightly doped in situ and subsequently implanted. ($\Delta V_{TN} \simeq$ 15 V at 10^6 rad.) Process A has a postrad subthreshold n-channel leakage current of less than 1 μA/mil; process B, of about 1 nA/mil. In addition, the sheet resistivity of the poly in all the three sublots was low. For A, ρ□ = 22 Ω/□f; for B, ρ□ = 42 Ω/□; and for C, ρ□ = 64 Ω/□.

Subsequent measurements of V_{TN} and V_{TP} across a diameter of two wafers from each lot showed wafers from process C (in situ plus implant) to have a grossly nonuniform distribution in threshold voltages. We conclude that these wafers had a gross nonuniformity in poly thickness, enabling the implanted phosphorus to penetrate the poly. This probably also explains the poor radiation hardness.

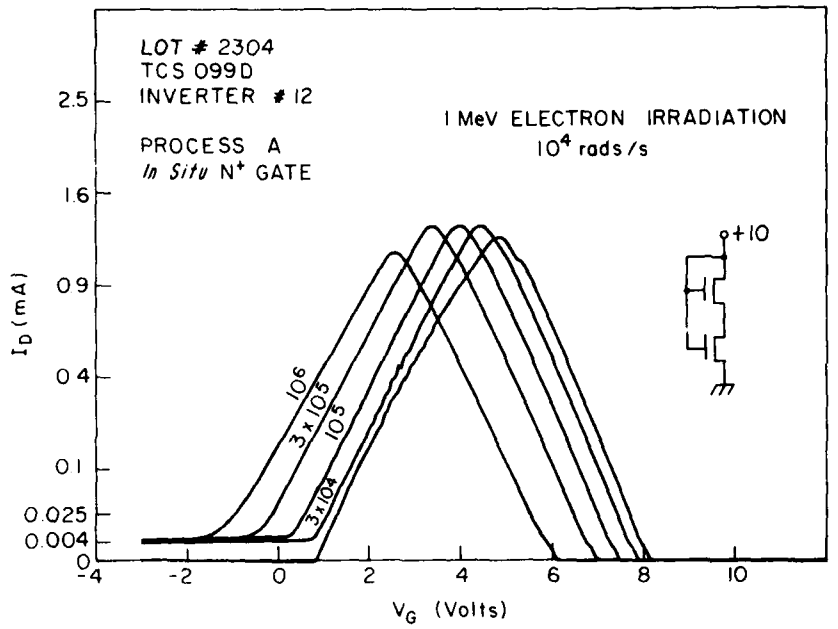


Figure 7. Pre- and postirradiation inverter characteristics, I_D vs V_G, process A. Parameters on curves are total dose in rad. (I_D plotted on square-root and log scales.)

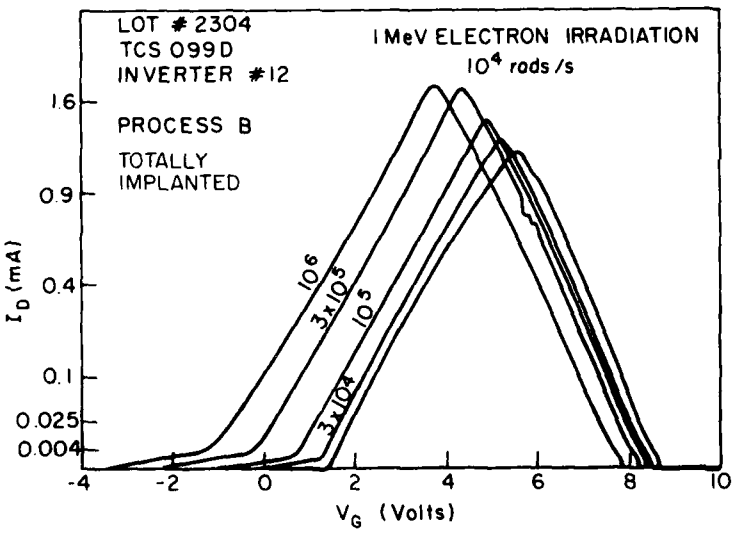


Figure 8. Pre- and postirradiation inverter characteristics, I_D vs V_G, process B. Parameters on curves are total dose in rad.

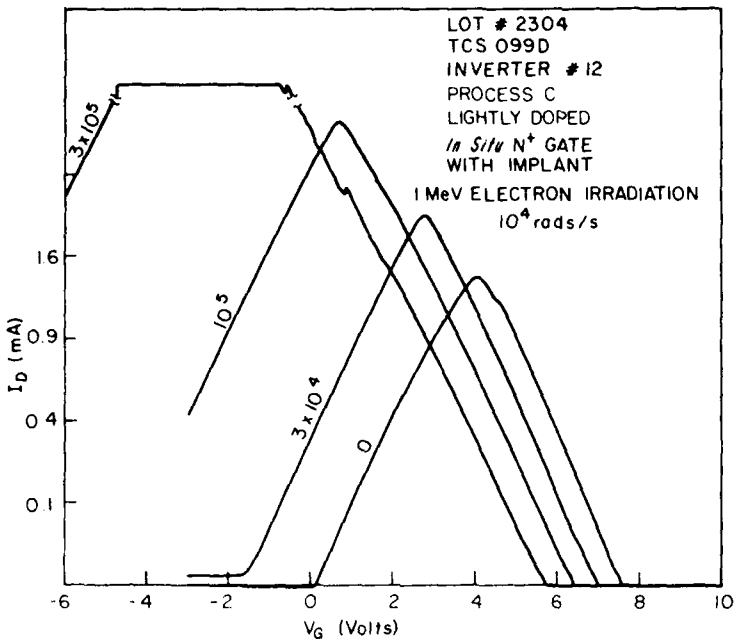


Figure 9. Pre- and postirradiation inverter characteristics, I_D vs V_G, process C. Parameters on curves are total dose in rad.

From these experiments we conclude that both in situ-doped poly and implanted poly can be used in a hardened process, although the sheet resistivity of in situ-doped poly is lower. The hardness of the implanted poly suggests that implanted LPCVD poly might be a good intermediate step to take before in situ-doped LPCVD poly becomes a reality. This would improve step-coverage yield and give a conductor with acceptable conductivity.

CONTROL OF BACK-CHANNEL LEAKAGE BY ION IMPLANTATION

One of the limiting factors in the use of CMOS/SOS in radiation environments is the postirradiation "back-channel" leakage caused by charge trapping in the sapphire. Although this leakage can be controlled by hydrogen firing of the sapphire, this method does not work 100% of the time. Another way to minimize this current is to heavily dope the silicon at the Si/sapphire interface by ion implantation. The following experiment illustrates the effectiveness of such a scheme.

One half of a lot was processed in the normal fashion, which for the p-island consists of two implantation steps followed by a 1050°C implant anneal. The other half of the lot was processed without the 1050°C anneal. The implant schedule for the p-island is as follows:

- 150 keV boron, $3x10^{11}$ cm^{-2}
- 35 keV boron, $2x10^{12}$ cm^{-2}

The 150-keV deep implant is to dope the Si/sapphire interface so heavily that back-channel leakage is suppressed. However, with the 1050°C anneal, this implant could get redistributed to the point where any benefits it was intended to have would be negated. The results of this experiment can be seen clearly in Figs. 10 and 11. Figure 10 shows inverter characteristics for an inverter before and after ^{60}Co irradiation to 10^6 rads. The curves are plotted on both a square-root and log scale to show different features of the curves. While these circuits can be classified as fairly hard in terms of threshold-voltage shift, there is a substantial increase in leakage current after irradiation. One component which dominates the n-channel device at 0 V is the edge leakage, noticeable as a "kink" in the I-V characteristic at 0 V. The other back-channel current is characterized by a nearly constant level from -1 V and below.

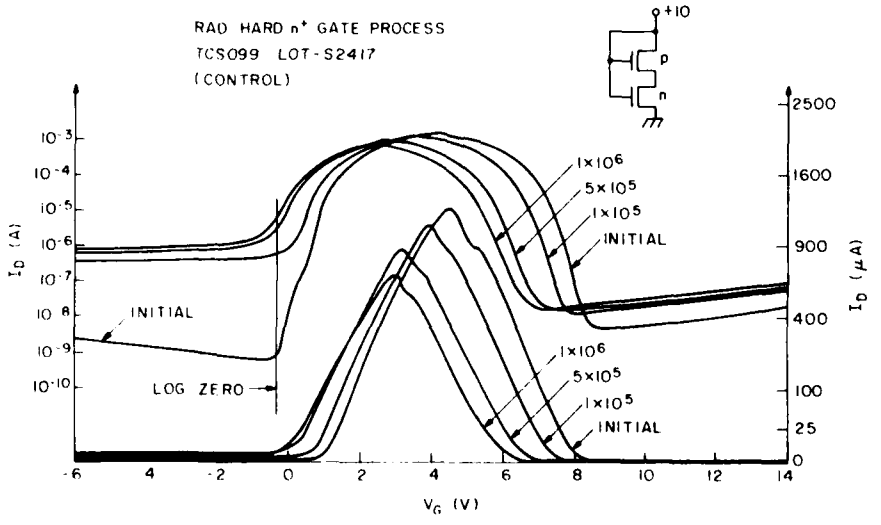


Figure 10. Pre- and postirradiation inverter characteristics for a normally processed wafer.

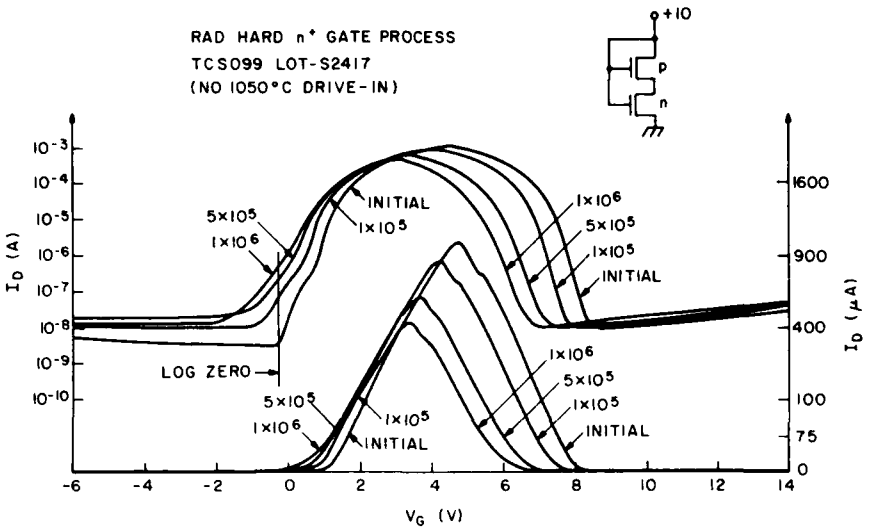


Figure 11. Pre- and postirradiation inverter characteristics for a wafer processed without the 1050°C implant drive-in.

Figure 11 shows the same type of curves from a wafer without a 1050°C anneal or drive-in. Here the edge leakage is still present, but the back-channel leakage is reduced by two orders of magnitude below that of the control (Fig. 10). While one experiment is by no means definitive, we are encouraged by the results.

E. EVALUATION OF BASELINE HARDENED PROCESS

The "bottom-line" in radiation hardness is determined by several things. With the n-channel device it is important that the initial threshold be low enough to preserve switching speed and noise immunity. After irradiation the threshold usually shifts in a negative direction, so that the important factor is whether the device "goes depletion" and draws large currents at $V_G = 0$ V. With the p-channel device the threshold also tends to shift in a negative direction under irradiation, so that the important postirradiation criterion is the magnitude of ΔV_{TP}; if ΔV_{TP} exceeds a certain value, switching speed and noise immunity will not be preserved.

With the CMOS/SOS process, control of initial threshold voltage is not as good as with bulk CMOS. Typically the CMOS/SOS process shows a "spread" in V_{TN} of about 0.7 V and a spread in V_{TP} of about 0.5 V. Thus, to optimize the process we can make V_{TP} as low as, say, 0.75 V. For the n-channel device we typically expect ΔV_{TN} to be less than 2.0 V after 10^6 rad of ionizing radiation. Thus setting V_{TN} = 2.0 V will result in having most n-channel transistors remain enhancement mode after irradiation. Note, however, that all this neglects subthreshold and edge leakage that may result in large currents at V_G = 0 V even with V_{TN} J 0 after irradiation. Simulations done on worst-case failure modes in a 1K RAM (TCS150) have shown that the circuit can tolerate 3 μA/mil of n-channel leakage at V_G = 0 V before it develops a soft error. Based on the above arguments one can establish the following criteria for radiation hardness:

TABLE 3. CRITERIA FOR RADIATION HARDNESS

n-channel: $I_{LN} \leq 3$ μA/mil to 10^6 rad (V_{TNO} = 2.0 V)
p-channel: $\Delta V_{TP} \leq 3$ V to 10^6 rad (V_{TPO} = 0.75 V)

The threshold shift criterion for the p-channel is based on observed maximum shifts and a guess at the maximum V_{TP} tolerable for high-speed operation. The summary of the radiation data is shown in Table 4.

Using the hardness criteria shown in Table 4, 45% (5/11 lots) are hard to 10^6 rad. Note, however, that the initial threshold voltages of the n-channel devices are nominally 1.0 V. This is too low for the present process. If we could adjust all the n-channel thresholds to 2.0 V, then the leakage current at 0 V would be quite different for some lots. With this revised threshold we find that 82% (9/11 lots) could be hard -- a quite acceptable figure.

The problem of the low initial threshold voltage can be fixed by increasing the doping of the p well. However, with SOS technology there is another problem regarding initial threshold voltages: the variability in initial threshold voltage from lot to lot. This is illustrated in Fig. 12 for the rad-hard n^+ and p^+ gate processes. Most of this variation appears to be due to defects in the starting material. Fortunately, a screening technique has been developed which significantly reduces this spread; we will be applying this procedure to try and minimize the spread.

TABLE 4. RAD-HARD n^+ GATE CMOS/SOS

Lot #	Type	V_{TNO}	V_{TPO}	$-\Delta V_{TN}$ (to 10^6 rad)	$-\Delta V_{TP}$ (to 10^6 rad)	Max I_{LN} (μA/mil) at V_G = 0 V (to 10^6 rad)	Max I_{LN} (μA/mil) at $V_G = V_{TNO} - 2.0$ V (to 10^6 rad)
2304	099	0.75	-1.80	0.9	2.15	10	2.5
2314	099	0.70	-1.65	0.40	1.30	15	0.1
2323	099	0.8	-1.70	2.0	2.20	30	3
2336	099	0.8	-1.70	2.0	2.10	30	3
2364	099	1.0	-1.80	0.45	1.50	0.20	0.001
2375	099	0.9	-1.90	1.20	2.0	3	0.1
2417	099	1.15	-2.20	1.00	2.10	1.5	0.3
2422	099	1.70	-1.20	1.15	1.0	1.0	0.8
2439	099	1.55	-2.40	2.15	2.40	20	0.10
2454	099	0.85	-1.50	4.45	1.85	1000	0.700
2521	121	1.05	-1.50	0.75	1.55	0.1	0.006

NOTE: All irradiations done on inverters with $V_G = V_{DD} = +10$ V, $V_{SS} = 0$ V.

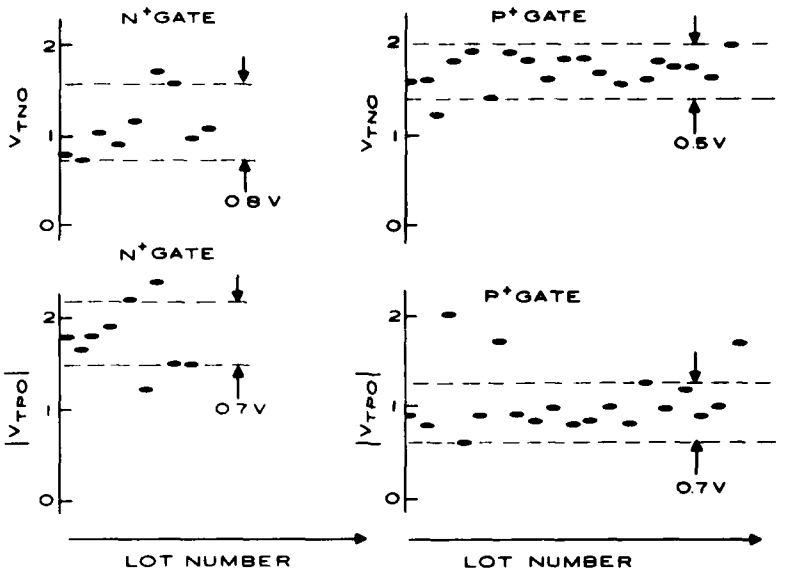


Figure 12. Initial threshold voltage uniformity (lot to lot) as a function of chronological order of processing (lot number).

F. ELECTRICAL TESTING OF 4K RAMs

In accordance with our program to develop a rad-hard n^+ gate process, the TCS191, CMOS/SOS, 4K memory was chosen as a viable candidate to demonstrate the feasibility of hardening a memory device by means of the present n^+ gate rad-hard process. The 191 is the original, unshrunk 5114, which is now being made at RCA Palm Beach Gardens (PBG) as a commercial product. The size reduction amounts to about 15%. The Appendix contains a publication by the RCA designers of the MWS 5114 that describes in detail the design of this memory. The 5114 contains 22,553 transistors in a 20-mm^2 area and is organized as 1024 4-bit words. This degree of complexity ensured that any success in hardening of the demonstration vehicle would provide a very strong case for achieving our contract objectives. Obviously, this approach could not be expected to achieve a reasonable yield of operational 4K memories, since the original design parameters did not take into account the requirements of a radiation environment.

All of the electrical testing was carried out on the Teradyne* memory tester, a very complex and expensive IC tester designed especially for testing memory devices. Three lots of the TCS191 were processed at SSTC, Somerville,

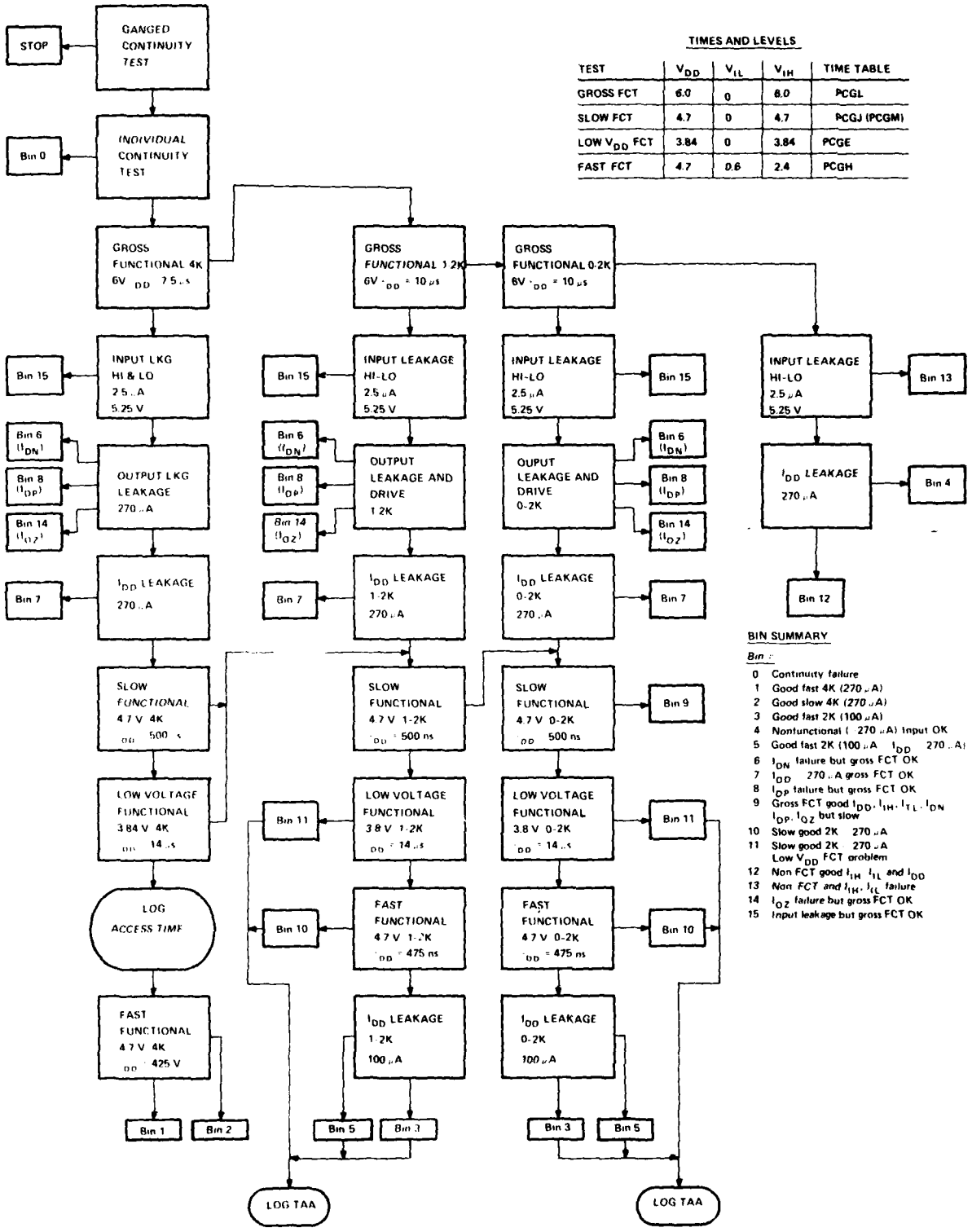
*Memory tester made by Teradyne Inc., Boston, MA.

and wafer probing of the three lots was carried out on the Teradyne tester, at Princeton, with the help of a test program originally designed to test the Palm Beach production device, namely, the MWS 5114 memory. Figure 13 is the flow chart of the test program. The original program was modified to perform tests at a voltage, V_{DD}, of 10 V (instead of the usual 5 V) and also to eliminate some of the program steps. The wafer-probing tests indicated that lot 2660 had nine potential 4K memories, lot 2581 had mostly 2K memories, and lot #2548 did not yield any type of operating device. Apparently some type of processing mistake had occurred during the fabrication of this lot. Four successful 4K memories were obtained from the potential nine samples from lot #2660 and one 4K from lot #2581. A new test program was written in place of the original program to conduct initial and postradiation measurements at the V_{DD} of 10 V.

G. RADIATION TESTING OF 4K RAMs

The ^{60}Co source located at RCA Somerville was used to expose the memory samples; then the samples were transported in a container of dry ice to the Laboratories at Princeton for measurement on the Teradyne tester. Devices which required exposures and measurements extending over several days were stored at dry-ice temperature. This technique guaranteed the continuity of the exposures, and the prevention of annealing during transportation and storage between exposures. In addition, six samples of the commercial product, MWS 5114, were tested at the same time and in the same manner as the TCS191 devices, but at a V_{DD} of 5 V. These test samples served as a good reference and clear demonstration of the hardness achieved in the rad-hard-processed TCS191 devices under the same test conditions of exposure to radiation and subsequent measurement. All samples were exposed with input and control lines high, and with a stored pattern during the exposure, which was random. A preferred pattern was probably established as the dose accumulated, since it has been shown that the inverters of the storage cell will tend to turn on in the same state as the dose accumulates and the threshold voltages shift.

Table 5 summarizes the results obtained with the five samples of the TCS191. We have listed the maximum standby leakage current and the access times measured with March, Address Complement, and Galpat test patterns as a function of dose. The program first used a March pattern for a gross functional test. If the device passed, it then used other patterns to carry out



TIMES AND LEVELS

TEST	V_{DD}	V_{IL}	V_{IH}	TIME TABLE
GROSS FCT	6.0	0	6.0	PCGL
SLOW FCT	4.7	0	4.7	PCGJ (PCGM)
LOW V_{DD} FCT	3.84	0	3.84	PCGE
FAST FCT	4.7	0.6	2.4	PCGH

BIN SUMMARY

Bin #

0 Continuity failure
1 Good fast 4K (270 µA)
2 Good slow 4K (270 µA)
3 Good fast 2K (100 µA)
4 Nonfunctional (270 µA) Input OK
5 Good fast 2K (100 µA I_{DD} 270 µA)
6 I_{DN} failure but gross FCT OK
7 I_{DD} 270 µA gross FCT OK
8 I_{DP} failure but gross FCT OK
9 Gross FCT good I_{DD}, I_{IH}, I_{IL}, I_{DN} I_{DP}, I_{OZ} but slow
10 Slow good 2K 270 µA
11 Slow good 2K 270 µA Low V_{DD} FCT problem
12 Non FCT good I_{IH} I_{IL} and I_{DD}
13 Non FCT and I_{IH}, I_{IL} failure
14 I_{OZ} failure but gross FCT OK
15 Input leakage but gross FCT OK

Figure 13. Flow chart of test program for 4K RAM.

TABLE 5. EFFECTS OF ^{60}Co IRRADIATION ON RAD-HARD TCS191, 4K MEMORIES PROCESSED AS n^+ GATE DEVICES

Lot (#) and Sample (No.)	Dose (krad)	Max Standby I_{DD} (μA)	March Access (ns)	Galpat Access (ns)	Address Complement Access (ns)
#2660					
No. 1	0	265	316	317	220
	10	2047	344	357	243
	50	2047	410	496	265
	100	366	300	308	226
	200	357	371	377	268
	500	334	572	577	384
	1000	Failed			
2	0	251	498	Not measured	325
	10	Failed			
	150	311	Not measured	Not measured	320
	300	Failed			
4	0	474	461	480	308
	10	1870	475	514	300
	50	Failed			
	150	548	451	500	301
	300	Failed			
6	0	298	362	383	247
	10	1912	376	429	255
	50	2047	396	470	270
	100	383	345	378	242
	200	369	449	449	274
	500	350	583	647	376
	1000	Failed			
#2581					
No. 10					
	0	492	307	308	221
	100	Failed			

additional functional tests and also various parametric measurements. Table 5 shows that samples 2 and 4 failed after (low) doses of 10 and 50 kilorads, respectively. However, both samples recovered and passed most of the tests after exposure to 150 krad. These samples failed once more after exposure to 300 krad, probably due to the growth of negatively charged interface states, which caused the n-channel threshold voltage to turn around and increase. Examination of the Teradyne test data indicates that samples No. 2 and 4 were only marginal devices before exposure. For example, No. 2 did not pass the Galpat or Walk tests, and No. 4 was slower than either No. 1 or 6, which turned out to be the hardest samples. As can also be seen from Table 5, the behavior of the leakage current correlates with the turn-about behavior of the n-channel threshold voltage. Failure levels range from 10^5 to 10^6 rad and are comparable to those of the TCS150, CMOS/SOS 1K memory, fabricated with the p^+ gate rad-hard process.

Six samples of the commercial product MWS 5114, 4K memory were irradiated at RCA Somerville and measured at RCA Laboratories in the manner described for the TCS191. These samples provided a sharp contrast with the rad-hard 191 samples, which were identical except for the size difference. Table 6 summarizes the results of the tests. The maximum standby leakage current and the access time measured with a March pattern are listed as a function of dose. The test program used in these tests was the standard program designed for the Palm Beach products. The standby current was measured for several test patterns, for example, checkerboard, checkerboard bar, all 0's, all 1's, alternate rows, alternate rows bar, alternate columns, and alternate columns bar. We have selected the maximum value independent of pattern. It can be seen that failure doses range from 8 to 12 krad, in contrast to the 100-1000 krad for the rad-hard 191 memories; thus, the hardness improves by at least an order of magnitude.

It appears, from the data of Table 5, that leakage current did not cause failure of the 191 memories, since the final values were not significantly larger than the initial values. This was not suprising, since the 191 storage cell utilizes a p-channel rather than an n-channel Read/Write transistor; the n type would have made it more sensitive to leakage current. Threshold voltage shifts were probably responsible for some of the storage-cell locations failing the functional test patterns. To obtain further insight into the failure mechanism and to classify the hardness of the three lots of memory devices,

TABLE 6. EFFECTS OF ^{60}Co IRRADIATION ON MWS 5114 4K MEMORIES MADE AT RCA PALM BEACH GARDENS WITH A COMMERCIAL n^+ GATE PROCESS

Sample No.	Dose (krad)	Max I_{DD} Standby (μa)	March, V_{cc} = 5 V Access Time (ns)
1	0	19	264
	4	42	310
	8	1027	383
	12	Failed	
2	0	6	241
	4		Not measured but passed gross functional test
	8	1749	265
	12	Failed	
3	0	10	228
	4	144	Not measured but passed gross functional test
	8	Failed	
4	0	33	289
	4	129	372
	8	696	418
	12	Failed	
5	0	13	279
	4	130	376
	8	1224	347
	12	Failed	
6	0	15	228
	4	159	286
	8	Failed	

inverter measurements were made with test devices contained on wafers of the processed lots. Each wafer contained two inverters; these were packaged and radiation-tested.

Table 7 summarizes the results by listing the mean, minimum, maximum, and σ of the inverter sample distributions of initial threshold voltage and voltage shifts as a function of cobalt-60 total dose. There were several samples that showed evidence of a turnabout in the n-channel threshold after about 500 krad, but in general this effect was not significant. Examination of these results indicates that inverters from lots #2660 and 2581, from which the 4K test samples originated, shifted into depletion after about 100 krad, whereas those from lot #2548 did not do so until a dose of 500 krad was achieved.

A similar set of measurements was made with inverters from wafers processed at RCA Palm Beach, and thus characteristic of the MWS 5114 memories. Table 8 lists these results for two lots and seven inverter samples for total doses of 4, 8, and 12 krad. The contrast of these results compared to those in Table 4 is very sharp and indicative of the hardness of the n^+ gate rad-hard process relative to the n^+ gate standard process. The dose ratio for a ΔV_{TN} of $\sim$1 V is about 100/6 for the worst-case lots of the rad-hard to standard process and 500/6 for the hardest lot of 191 memories.

It is interesting to examine the inverter results and to predict the hardness failure levels of the 191 and 5114 memories. Table 9 lists the memory samples, their failure doses, and the corresponding threshold voltages, shifts, and penetration into the depletion region predicted by the inverter measurements. The leakage current determined at 0 V is also listed. In the case of 191, the data obtained with inverters from wafers which supplied the test samples (except for wafer No. 4) were used in the table. In this latter case, no inverters were available for evaluation. As a comparison, Table 10 lists the same data but with threshold voltages, shifts, and leakage currents all based on the mean inverter values from Table 7. It can be seen that the mean representation of the lot characteristics is fairly good, relative to shifts and depletion-region penetration. This means that for a hardness assurance program, it appears that an average representation of the lot hardness may be adequate. Obviously, this is still a small sample test, and it requires a large number of tests before a definite conclusion can be drawn.

TABLE 7. MEAN, MINIMUM, MAXIMUM, AND σ VALUES OF INITIAL THRESHOLD VOLTAGE AND VOLTAGE SHIFTS FOR INVERTER SAMPLES FROM TCS191 LOTS IRRADIATED BY ^{60}Co

Lot (#)	Value	V_{TN} 0 krad	$-\Delta V_{TN}$ 100 krad	200 krad	500 krad	1000 krad
#2660						
7 Wafers	Mean	1.0	1.1	1.6	2.3	2.5
10 Samples	Min	0.9	0.7	0.9	1.3	1.5
	Max	1.2	1.6	2.5	3.6	4.0
	σ	0.1	0.3	0.6	0.8	0.8
#2581						
10 Wafers	Mean	0.9	1.2	2.0	3.2	3.5
12 Samples	Min	0.8	0.7	1.2	1.9	1.5
	Max	1.1	2.2	3.4	5.3	5.8
	σ	0.1	0.4	0.6	0.9	1.1
#2548						
4 Wafers	Mean	0.9	0.5	0.8	1.2	1.6
6 Samples	Min	0.9	0.3	0.6	0.9	1.4
	Max	1.0	0.6	0.9	1.5	2.0
	σ	0.1	0.1	0.1	0.2	0.2
			$-V_{TP}$	$-\Delta V_{TP}$		
#2660						
	Mean	1.7	0.7	0.9	1.4	1.8
	Min	1.5	0.6	0.8	1.3	1.1
	Max	1.9	0.7	1.0	1.5	2.0
	σ	0.1	0.1	0.1	0.1	0.3
#2581						
	Mean	1.8	0.6	0.8	1.3	1.7
	Min	1.6	0.5	0.7	1.1	1.5
	Max	1.8	0.6	1.0	1.6	2.2
	σ	0.3	0.1	0.1	0.1	0.2
#2548						
	Mean	1.7	0.5	0.8	1.3	1.7
	Min	1.6	0.4	0.6	1.2	1.7
	Max	1.9	0.7	1.0	1.4	1.8
	σ	0.1	0.1	0.2	0.1	0.1

TABLE 8. VALUES OF INITIAL THRESHOLD VOLTAGES AND VOLTAGE SHIFTS OF INVERTER SAMPLES FROM 5114 LOTS IRRADIATED WITH ^{60}Co

No. of Samples	Value	V_{TN} 0 krad	$-\Delta V_{TN}$ 4 krad	$-\Delta V_{TN}$ 8 krad	$-\Delta V_{TN}$ 12 krad
7	Mean	1.1	0.5	1.3	2.4
	Min	1.0	0.3	1.0	2.0
	Max	1.2	0.9	1.7	3.2
	σ	0.1	0.2	0.3	0.4
		$-V_{TP}$	$-\Delta V_{TP}$		
	Mean	1.0	0.4	0.6	0.9
	Min	0.8	0.1	0.3	0.5
	Max	1.1	0.7	1.0	1.4
	σ	0.1	0.2	0.3	0.3

The results indicate that the 191 rad-hard memories failed because of threshold-voltage shifts, rather than because of leakage-current increases. This was probably due to the use of a p-channel (instead of n-channel) Read/Write transistor for accessing the storage cell inverter. By the same token, the p-channel shifts combined with any turn-about in n-channel thresholds would slow the devices, so that they would fail because of speed considerations as well. The access time shown in Table 5 first decreased, then finally increased, prior to failure; the ΔV_{TP} shifts dominated the access time. The inverter results show that a failure criterion based on nonpenetration of the depletion region may be too severe, since the memory samples failed with penetrations in the range of 0.3-1.7 V. This fact, however, may be unique to this particular memory design and not necessarily a general result. A similar conclusion can be deduced from the 5114 data. The depletion voltage ranged from 0.2 to 1.3 V. There was one basic difference between the two sets of measurements: namely, V_{DD} was 10 V for the 191, compared to 5 V for the 5114 memories. Thus, the voltage difference would allow for greater tolerance to voltage shifts. The imposition of a failure criterion of $V_{TNO} - \Delta V_{TN} \geq 0$ would have predicted approximate failure doses for the 191 and 5114 samples, respectively, that

TABLE 9. FAILURE DOSE, SHIFTS, AND LEAKAGE CURRENT SFOR 191 AND 5114 SAMPLES, BASED ON SPECIFIC WAFER INVERTERS WHERE POSSIBLE

Sample No. (Lot #)	Type	Wafer	Mean Failure Dose (krad)	V_{TN}	ΔV_{TN}	$-V_{TP}$	$-\Delta V_{TP}$	I_{DD} (μA/mil)	Depletion Voltage
1 (2660)	191	3	750	1.2	2.3	1.5	1.8	2000	1.1
2 (2660)		3	225	1.2	1.6	1.5	1.0	788	0.4
4 (2660)		4	225	.....	No inverter data	.....			
6 (2660)		9	750	1.1	2.8	1.5	1.7	4000	1.7
10 (2581)		12	100	1.0	1.3	1.6	0.6	20	0.3
3 and 6	5114	--	8	1.1	1.3	1.0	0.6	20	0.2
1, 2, 4, and 5		--	12	1.1	2.4	1.0	0.9	189	1.3

TABLE 10. FAILURE DOSES, SHIFTS, AND LEAKAGE CURRENTS FOR 191 SAMPLES BASED ON MEAN LOT VALUES OF INVERTER RESULTS

Sample No. (Lot #)	Mean Failure Dose (krad)	V_{TN}	$-\Delta V_{TN}$	$-V_{TP}$	$-\Delta WV_{TP}$	I_{DD} (μA/mil)	Depletion Voltage
1 (2660)	750	1.0	2.4	1.7	1.6	900	1.4
2 (2660)	225	1.0	1.6	1.7	0.9	488	0.6
4 (2660)	225	1.0	1.6	1.7	0.9	488	0.6
6 (2660)	750	1.0	2.4	1.7	1.6	900	1.4
10 (2581)	100	0.9	1.2	1.8	0.6	157	0.3

correspond to the data shown in Table 11. Thus, it appears that the criterion would allow a prediction good within a factor of ∿2-10 of the actual failure doses for the 191 and a factor of ∿2 for the 5114.

It can be concluded that these test results demonstrate the feasibility of hardening SOS memories by the use of the present n^+ gate rad-hardened process without the aid of rad-hard circuit design, to achieve total-dose capability in the range of 10^5-10^6 rad.

TABLE 11. PREDICTED FAILURE DOSE FOR 191 AND FOR 5114 SAMPLES, BASED ON THE CRITERION OF $V_{TNO} - \Delta V_{TN} \geq 0$

Sample No.	Device	Failure Dose (krad)	Experimental Failure Dose (krad)
1	191	135	750
2	191	135	225
6	191	80	750
10	191	70	100
1,2,3,4,5	5114	7	8-12

SECTION IV

CONCLUSION

We have demonstrated the feasibility of using an n^+ phosphorus-doped polysilicon-gate technology to build radiation-hardened integrated circuits. In particular it was shown that a commercial 4K SOS RAM can be hardened to a level of 5×10^5 rad by the use of hardened processing techniques alone.

This is a significant improvement in the state of the art, since the use of n^+ gate technology will allow fabrication of higher-speed parts (because of the low sheet resistivity of polysilicon), presumably without the room-temperature bias instability problems experienced with hardened p^+ gate processes. In addition we have shown that we were able to achieve this level of hardness for the 4K RAM without having to use any hardened design rules. This opens up the possibility of hardening already existing LSI chips heretofore available only as commercial parts, and thereby circumvents the costly and time-consuming task of designing a custom chip for rad-hard applications.

Circuit-probe yields are still low with this process, but this is caused mainly by the lack of a hardened low-temperature reflow for the field oxide. Fortunately RCA has recently done independent work in this area and has nearly completed development of a fully hardened low-temperature reflow process. Completion of this development effort should allow the fabrication of hardened CMOS/SOS parts with circuit-probe yields comparable to those of commercial processes.

The increase in n-channel leakage during irradiation is usually thought to be the major cause of failure of CMOS circuits. However, these parts apparently failed for other reasons (probably excessive p-channel Read/Write transistor shifts). Thus we may conclude that if n-channel Read/Write transistors were used, this design would be even more radiation tolerant than the design actually measured. In Section III.D we have shown that postirradiation back-channel leakage current can be suppressed by ion implantation of the back interface. Previous work at RCA has also shown that it is possible to suppress edge leakage in n-channel MOS/SOS transistors by implantation of island edges [3]. Application of these techniques could provide solutions to our most severe radiation problems at the present time.

The results of Section III.E suggest that the prospects of maintaining a hardened n^+ gate process on a given wafer processing line are good. If we can

control initial n-channel thresholds and keep them at approximately 2 V, about 80% of all the lots processed would be hard even without solving the leakage-current problem. Suppressing back-channel and edge leakage can only increase this number.

The problems remaining to be solved are not trivial. Nevertheless they are problems for which we have reasonable solutions. Predictions of future progress are always risky, but from our vantage point, it appears that solutions to the major hardening problems of CMOS/SOS are well within reach.

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APPENDIX

A CMOS/SOS 4K Static RAM

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Abstract—**High density CMOS/SOS technology has been used to develop a fully static 4096-bit RAM with a five-transistor storage cell. Selection of a five-transistor memory cell has reduced the access to the flip-flop storage element to a single word line transistor and bit line. The word line transistor must be able to prevent data altering currents from entering the memory cell at all times except for the write operation. The control of the word line transistor current conduction involves creation of an operation-dependent bias voltage which, when applied to the transistor gate, modulates the maximum allowable current into or out of the storage cell. The write operation is enhanced by reducing the bias voltage across the memory cell, thereby making the current needed to alter the cell smaller.**

Through the use of a 5 μm design rule, the memory cell occupies 2913 μm^2. The 4096-bit static CMOS/SOS RAM contains 22 553 transistors in 20 mm^2. Organized as 1024 4-bit words, the 4096-bit RAM has a read cycle time of 350 ns and standby power dissipation of 50 μW at V_{cc} = 5 V and temperature of 27°C.

I. Introduction

A STATIC 4096-bit CMOS RAM can result in significant system advantages with high-speed operations at extremely low power dissipation levels. CMOS memories have previously been plagued by large chip sizes when compared to silicon gate NMOS designs of equivalent bit capacity and design rules. Through the use of a five-transistor static storage cell, efficient decoding and control logic schemes, and employing silicon on sapphire (SOS) technology, a static 4096-bit CMOS RAM can be achieved which compares quite favorably in die area yet consumes only a fraction of the power dissipated by NMOS counterparts [1].

II. Five-Transistor CMOS Memory Cell

In order to reduce the area of the static memory cell, a five-transistor memory cell was selected [2]. A five-transistor cell eliminates the need for one word line transistor and bit line contact as part of the more conventional six-transistor cell [3], [4] thereby reducing the cell area. The use of only one transmission gate and a single bit line for accessing the cell results in a unique set of requirements for the decoding and control logic.

The five-transistor cell which was selected is shown in Fig. 1(a). The $P1$, $P2$, $N1$, and $N2$ devices comprise the cross-coupled inverter, which is the storage element. The $P3$ device is the transmission gate which is used to connect the flip-flop to the bit lines and transfer data into or out of the cell. Of primary importance in the design of a memory using the five-transistor cell is to guarantee that there are no false data conditions due to read or write sequences. The memory cell must therefore be a stable storage element.

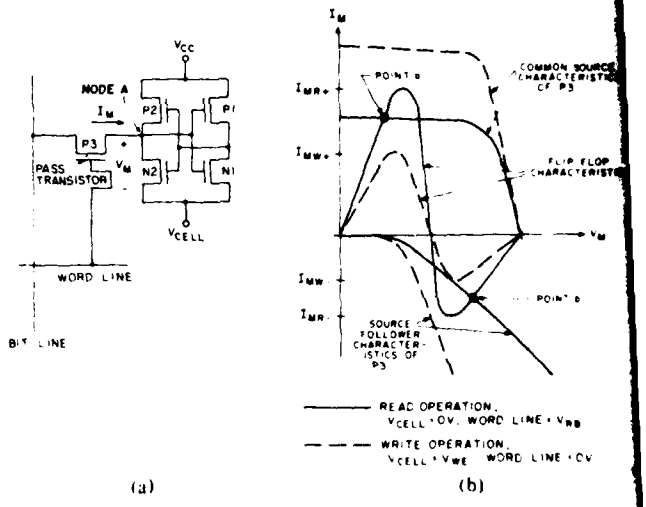

Fig. 1. (a) Five-transistor CMOS memory cell. (b) Current-voltage characteristics of flip-flop and word line transistor.

When using the five-transistor cell in an array of cells so that many cells share bit and word lines, there are two modes of possible false data that must be considered. The first case involves multiple cell selection in which two or more cells sharing a bit line have their respective word lines enabled. In this case, the signals that are subsequently transferred to the bit line must not be able to alter the contents of any cell. It is possible to design a decoder which will ensure that all word lines are fully disabled before selection of a word line, but this "break before make" decoding scheme adds complexity to the decode and control logic.

The second case to be considered involves bit line voltage in the form of charged parasitic line capacitance which could alter the data in a cell when the word line is enabled. The bit line capacitance, which is charged to the opposite state to that at the input node of the selected cell, could provide sufficient charge to dump back into the cell and force the flip-flop to change state (assuming that the total bit line capacitance is much greater than the input capacitance of an individual cell).

In both cases that have been presented, the five-transistor cell design would result in a stable storage element if the dc impedance presented by the word line transistor is made large enough so that sufficient current to change the state of the cell could not pass from the bit line to the flip-flop. However, this would result in a cell that cannot be written into. This apparent paradox is resolved using bias voltage levels on the

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word lines and for the power supply to the cell which are tailored for the read and write operations to ensure safe reading and a complete write operation.

The read operation involves applying the proper bias voltage level to the word line so that the impedance of the word line transistor is high enough to prevent current, which is capable of altering the cell, from entering the cell from the bit line. As the impedance of this transistor is increased, the current which the cell can provide for reading is reduced and the read operation speed is slowed. It was a design goal to optimize the word line bias during the read operation so as to yield the highest speed response and yet not jeopardize the cell stability.

A quantitative analysis can be performed by calculating the current necessary to change the cell state and comparing this with the conduction properties of the word line transistor being the parameter of interest. Through the use of computer modeling (R-CAP) [5], a plot of the flip-flop and word line transistor characteristics can be generated. This is shown in Fig. 1(b) in which I_M is the current flowing into the flip-flop or through the word line transistor as a function of V_M, the voltage at the common node of a $P2/N2$ drain and a $P3$ drain/source. Depending upon the state of the bit line, node A can either be the drain or the source of $P3$, and the current conducted by $P3$ into the flip-flop will depend upon the state of the bit line. The word line transistor $P3$ will act in either the common source or source follower mode of operation with regard to node A. Both modes of operation of the $P3$ device are shown in Fig. 1(b). In order to guarantee a safe read, the worst case conditions will be calculated for the bit line fixed at V_{cc} and ground.

If, for example, the bit line is held at V_{cc} and the word line is enabled with some potential which turns $P3$ on, the flip-flop with a ground potential at node A will change state only if current in excess of I_{MR+} can be provided through $P3$. In Fig. 1(b), point "a" is the intersection of the flip-flop characteristic with the common source load line of $P3$ for a word line voltage of V_{RB}. Conversely, for the bit line grounded and the word line at V_{RB}, the current necessary to drive the cell from V_{cc} at node A is I_{MR-} which is prevented by the intersection of the $P3$ load line with the flip-flop characteristics at point "b." For the read operation, it is necessary to maximize the I_{MR+} and I_{MR-} values in order to increase the charging current for sensing the data. This is accomplished by fixing V_{CELL} at ground potential, therefore placing the full V_{cc} across the cell. With 5 μm channel width for $P1$, $P2$, and $N1$, 12 μm for $N2$, 33 μm for $P3$, and 5 μm length for all devices, typical values for V_{cc} = 5.0 V are I_{MR+} = 650 μA and I_{MR-} = 200 μA at 27°C.

For the write operation, the impedance of $P3$ is reduced by driving the word line to ground, thereby permitting current in excess of I_{MR+} and I_{MR-} to flow. This condition allows bit line data to be loaded into the flip-flop. In order to enhance the write operation in terms of speed and safety margin, the potential across the flip-flop is reduced by driving V_{CELL} to a positive voltage above ground. Increasing V_{CELL} above ground reduces the flip-flop current peaks to I_{MW+} and I_{MW-} in Fig. 1(b). The write enhancement gained by raising V_{CELL} is especially important for V_{cc} values less than 5 V in terms of the write time response of the flip-flop. The V_{CELL} value for V_{cc} = 5.0 V is selected to be 1.7 V which results in typical values of I_{MW+} = 50 μA and I_{MW-} = -15 μA at 27°C.

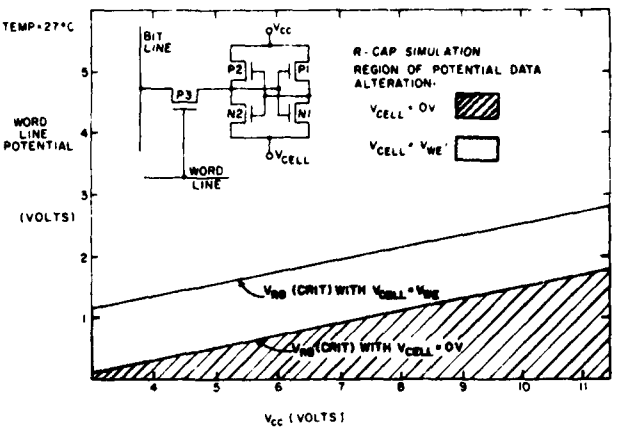

Fig. 2. Calculated critical word line potential limits [V_{RB}(CRIT)].

Selection of the V_{RB} voltage, which is applied to the word line during the read operation, must result in the intersection of the $P3$ load lines with flip-flop characteristics at points "a" and "b" in Fig. 1(b). The V_{RB} voltage for a particular V_{cc} is determined by finding the critical word line voltage V_{RB}(CRIT) which yields maximum $P3$ current without exceeding I_{MR+} or I_{MR-}. In Fig. 2, a plot of word line potential as a function of V_{cc} has been obtained by computer-aided calculations (R-CAP). The V_{RB}(CRIT) is shown for both V_{CELL} = 0 V, which is the case for reading, and V_{CELL} = V_{WE}, which is for the write operation. The limits shown in Fig. 2, *therefore, define the boundaries below which the word line* voltage could force a false data change. It is clear that, for V_{CELL} and the word line potential both at ground, the flip-flop is capable of being altered for V_{cc} = 3-12 V. Increasing V_{CELL} = V_{WE} during writing simply increases the design margin for a safe write and results in a faster write since a smaller current is necessary to flip the cell.

III. Word Line Bias Generator

A bias generator is required to produce the optimum V_{RB} which lies above the critical word line limit for V_{CELL} = 0 V as shown in Fig. 2[6]. The ideal situation would be a bias generator with an output voltage more positive than the critical limit by an amount representing the design margin (500 mV) and with the same slope as the V_{RB}(CRIT) versus V_{cc} limit with V_{CELL} = 0 V in Fig. 2. Fig. 3 shows the calculated and measured response of the bias generator circuit. The inset in Fig. 3 gives the schematic drawing of the circuit. The generator uses three depletion mode PMOS transistors in a voltage divider arrangement. The $P4/N1$ self-biased inverter subtracts V_{THP} + ΔV from the potential at node A where V_{THP} = PMOS threshold voltage and ΔV is the built-in voltage offset created by the current ratio of the self-biased inverter devices. The output response F, which is switched to the word line by decoding circuitry, matches the requirements for the V_{RB} voltage as seen by comparing the responses in Fig. 3 with the limit shown in Fig. 2. Variations in device parameters

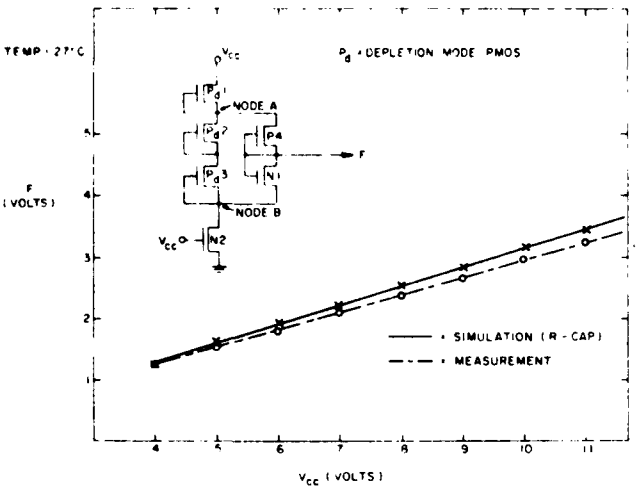

Fig. 3. Word line bias generator response.

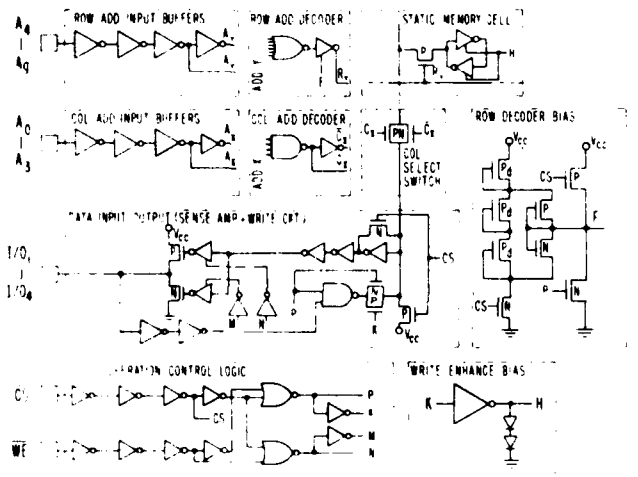

Fig. 4. 4096-bit CMOS/SOS static RAM circuit design.

are compensated by the bias generator in that as V_{THP} drops, the V_{RB}(CRIT) increases since $P3$ becomes more conductive. The bias generator output F increases as V_{THP} drops, which is in the proper direction. This is seen in the relationship governing the generator response:

$$F = \tfrac{2}{3} V_{cc} - |V_{THP}| - \Delta V.$$

The case where V_{THP} increases causes V_{RB}(CRIT) to decrease since $P3$ is less conductive. The output F will therefore decrease.

IV. Circuit Design

The five-transistor cell used in conjunction with the bias generator shown in Fig. 3 results in a high performance 4096-bit RAM with simple static decode and control logic. There is no need for bit line precharge or "break before make" decoder schemes. The full circuit schematic is displayed in Fig. 4. All logic elements are fully static CMOS gate configurations. The write enhance bias output H provides the V_{CELL} potential to the memory array during the write operation, in which case H

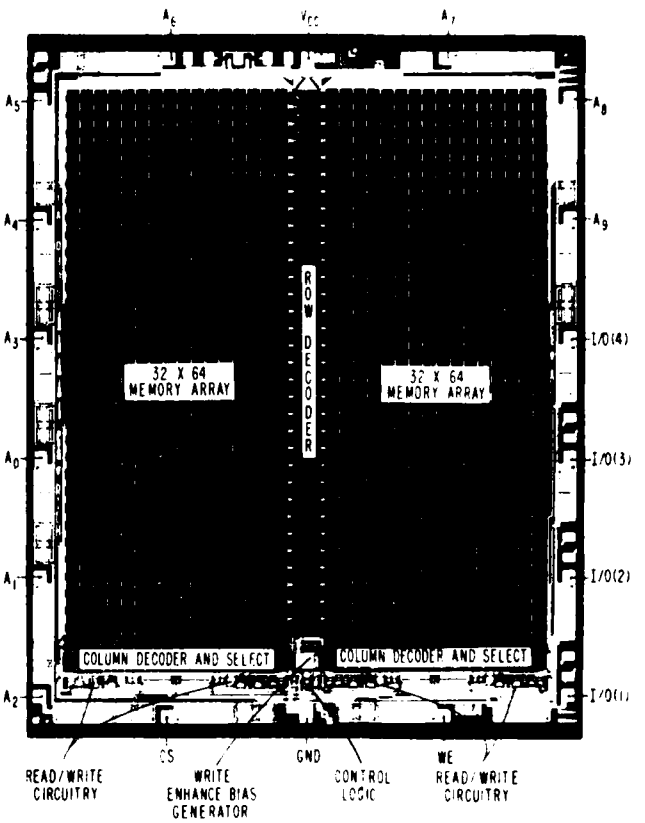

Fig. 5. Photomicrograph of 4096-bit CMOS SOS static RAM.

rises to approximately two forward-biased diode drops above ground. The sense amplifier circuit utilizes a self-biased CMOS inverter amplifier which has the high gain switching point weighted at approximately $V_{cc} - V_{THP}$. The critical data read path is controlled by the case where the word line transistor in the memory cell acts in the source-follower mode of operation. This occurs when the cell attempts to pull the bit line toward ground. The source-follower action of the word line device will result in a slower bit response than reading out a V_{cc} potential from the flip-flop. The sense amplifier must respond to slight drops in the bit line below V_{cc} in order to result in fast data access.

The 4096-bit RAM is organized as 1024 4-bit words and is pin-compatible with the industry standard 2114 part. The memory is fully static, requiring no $\overline{CS}$ clocking prior to each cycle. The memory operates for V_{cc} values of 3 to 12 V and over the temperature range of −55 to 125°C. All inputs and outputs are TTL compatible at $V_{cc} = 5$ V.

V. Chip Layout

The 4096-bit static RAM is laid out with 5 μm design rules for the eight-mask silicon gate CMOS SOS fabrication technology. This process results in enhancement mode PMOS and NMOS with threshold voltages of −0.9 and 1.1 V, respectively, and depletion mode PMOS with a threshold of 0.5 V. The five-transistor memory cell lays out in 293.3 μm². The total chip size is 4.0 × 5.0 mm with the memory cells occupying

60 percent of the total chip area. This high efficiency of memory area to total chip area is attributed to the simple static decoding and control logic that is used. The chip contains 13 360 PMOS and 9193 NMOS transistors with the static memory cells using 90.8 percent of the devices.

A photomicrograph of the completed 4096-bit RAM is shown in Fig. 5. The layout splits the 4096 memory cells into two blocks of 32 × 64 with the row decoder situated in the middle. The control logic and input/output circuitry are located adjacent to the column decoder and selection switches so as to minimize the loading effects upon the bit line after being switched through to the sense amplifier.

VI. Performance

The basic timing requirements for the 4096-bit CMOS/SOS RAM are displayed in Fig. 6. The $\overline{CS}$ input can be operated asynchronously with respect to the address inputs and is essentially used to enable/disable the data read and write circuitry and bias generators.

The word line bias generator output F is shown in Fig. 7. During the read operation, F = 1.5 V for V_{cc} = 5.0 V, which is the value shown in Fig. 3 and is well above the V_{RB}(CRIT) shown in Fig. 2 for V_{CELL} = 0 V. This bias arrangement has resulted in safe and stable data access when the 4096-bit RAM is subjected to rigorous read write pattern sensitivity tests such as walking and galloping ones and zeros. In Fig. 7, the F output can be seen to return to V_{cc} when $\overline{CS}$ = logic 1. F is driven to ground when CS and $\overline{WE}$ are both at logic 0 state (write operation) which successfully reduces the word line transistor impedance to allow for writing data into the selected cell.

The response of the write enhance bias generator H is seen in Fig. 8. This potential, which is directly connected to the V_{CELL} node of each memory cell, is seen to be 0 V at all times except when CS and $\overline{WE}$ equal logic 0 (write operation), at which time the H output rises to 1.75 V for V_{cc} = 5.0 V. There is no difficulty in the write enhance bias generator maintaining the voltages shown in Fig. 8 for all 4096 cells since CMOS memory cells, such as the five-transistor cell in Fig. 1, consume no dc current except for leakage currents (which are typically less than 500 pA/cell at V_{cc} = 5.0 V). The write enhance generator only has to sink transient currents during the time the cells are switching state or when the input node of the flip-flop (node A in Fig. 1) rises momentarily above the ground when reading out a 0 with a bit line previously charged near V_{cc}. These transient currents are no more than approximately 200 μA at V_{cc} = 5.0 V.

The worst case read access time can be seen in Figs. 9 and 10. The pattern used reads data from word 15 by maintaining a word line with data which is opposite to that in the previous operation. The read access time for word 15 is a measure of the response of the column decoder, the bit line interaction with the sense amplifier, and the propagation of data from the sense amplifier through the output drivers. The read logic 1 access is 175 ns and the read 0 access is 150 ns for V_{cc} = 5.0 V, as seen in Figs. 9 and 10, respectively.

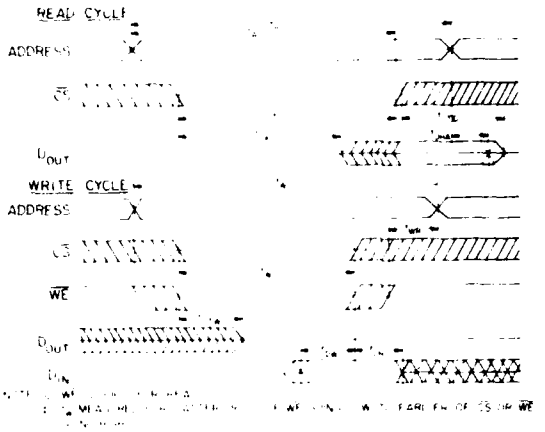

Fig. 6. Basic timing requirements for 4096-bit static RAM.

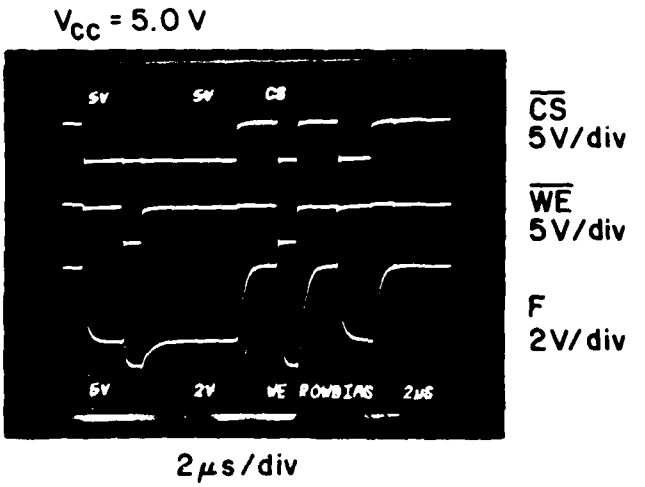

Fig. 7. Word line bias generator measured response.

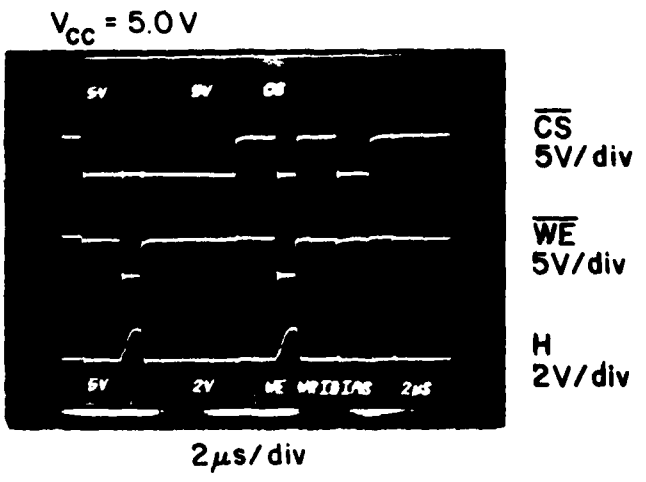

Fig. 8. Write enhance bias generator measured response.

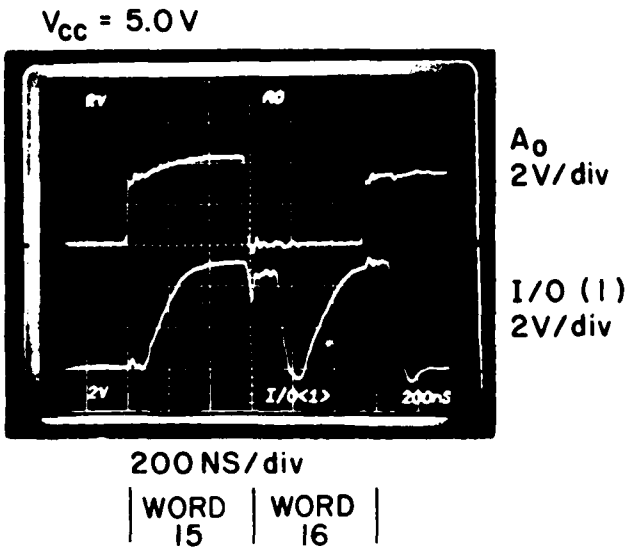

Fig. 9. Worst case read access time response (READ 1) TEMP = 27°C.

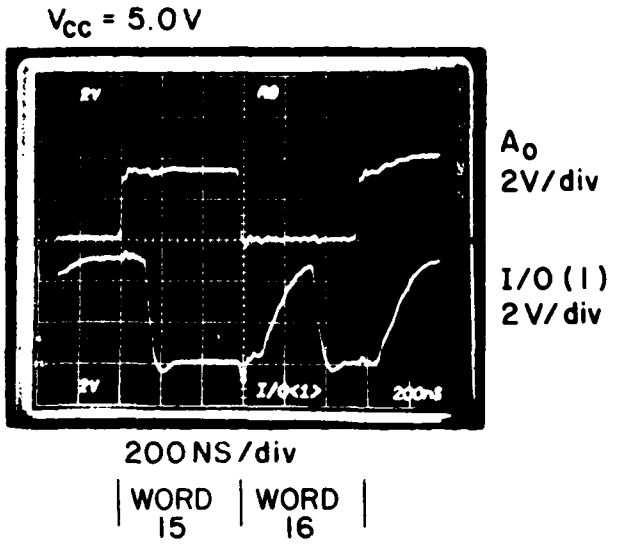

Fig. 10. Worst case read access time response (READ 0) TEMP = 27°C.

Reading word 16 in Figs. 9 and 10 is, however, the worst case since the pattern used senses the same data as in word 15 from the previous cycle (a logic 1 in Fig. 9 and a logic 0 in Fig. 10), except that changing to word 16 not only moves to a new bit line, but also to a new word line. The new bit line selected was charged to a logic 0 and logic 1 in Figs. 9 and 10, respectively, when reading word 15 so that moving to a new word line which intersects a cell that contains the complementary data forces the memory cell of word 16 to pull the bit line to the opposite state. Reading word 16 measures the row decoder ability to select a cell, the response of the cell to change the data on the bit line, and the sensing and transferring of data to the output. In both Figs. 9 and 10, the output responds to the selection of the charged bit line from the previous cycle before enabling the pass transistor with the subsequent data response of the selected cell.

The worst case access time at V_{cc} = 5.0 V is seen as 350 ns for both read logic 1 and logic 0.

VII. Conclusions

A five-transistor memory cell has been successfully used in the design of a 4096-bit static CMOS/SOS RAM. Proper control of the word line potential results in a stable storage element with fast data access. Simple static control logic that is used permits 60 percent efficiency of memory area to total chip area. CMOS logic for low power and high speed and SOS technology for packing density and reduced parasitic capacitance has resulted in a 4096-bit static RAM occupying 20 mm^2 with a read access time of 350 ns and standby power dissipation of 50 μW at V_{cc} = 5 V.

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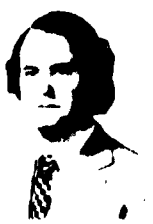

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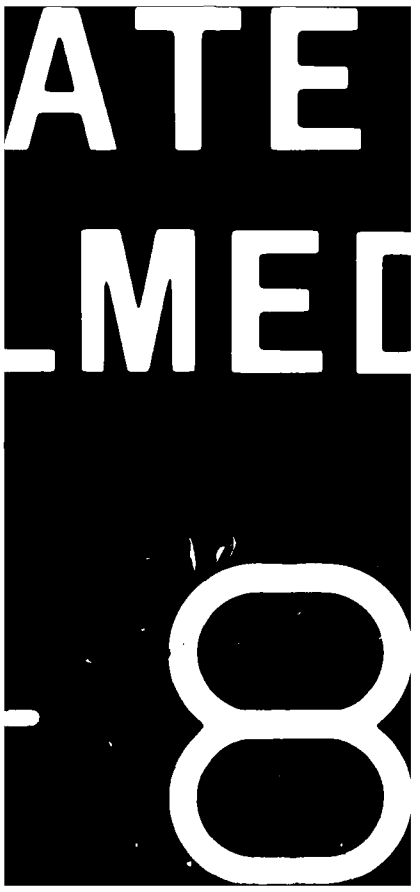
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